UNIVERSITY OF CAMBRIDGE

Lynx: Using OS and Hardware Support for Fast Fine-Grained Inter-Core Communication

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Computer Laboratory

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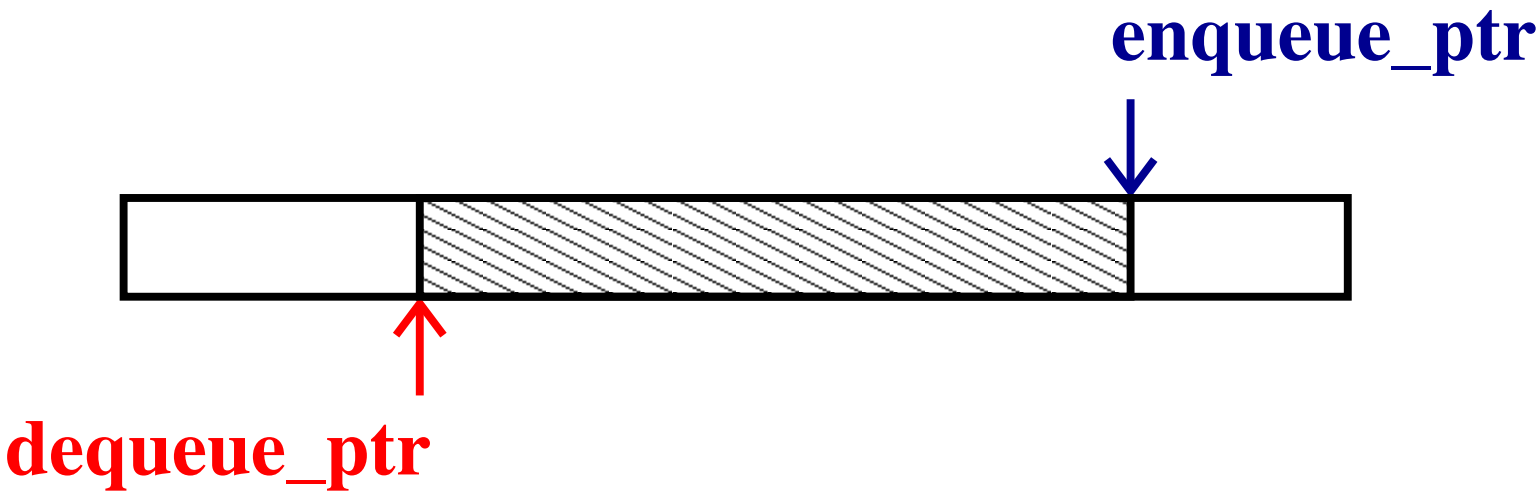
Outline

- Background:
  - Lamport's queue
  - Multi-section queue
- Lynx queue
- Performance evaluation

Lamport's Queue Bottlenecks



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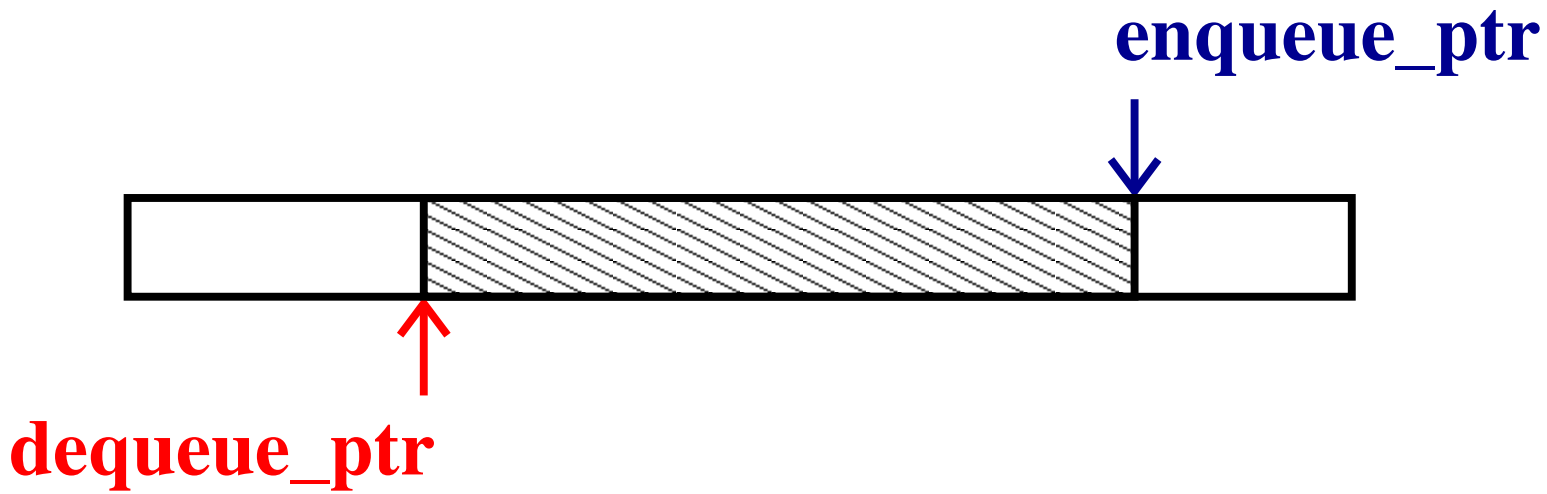


```
while(next_enqueue_ptr == dequeue_ptr){;}
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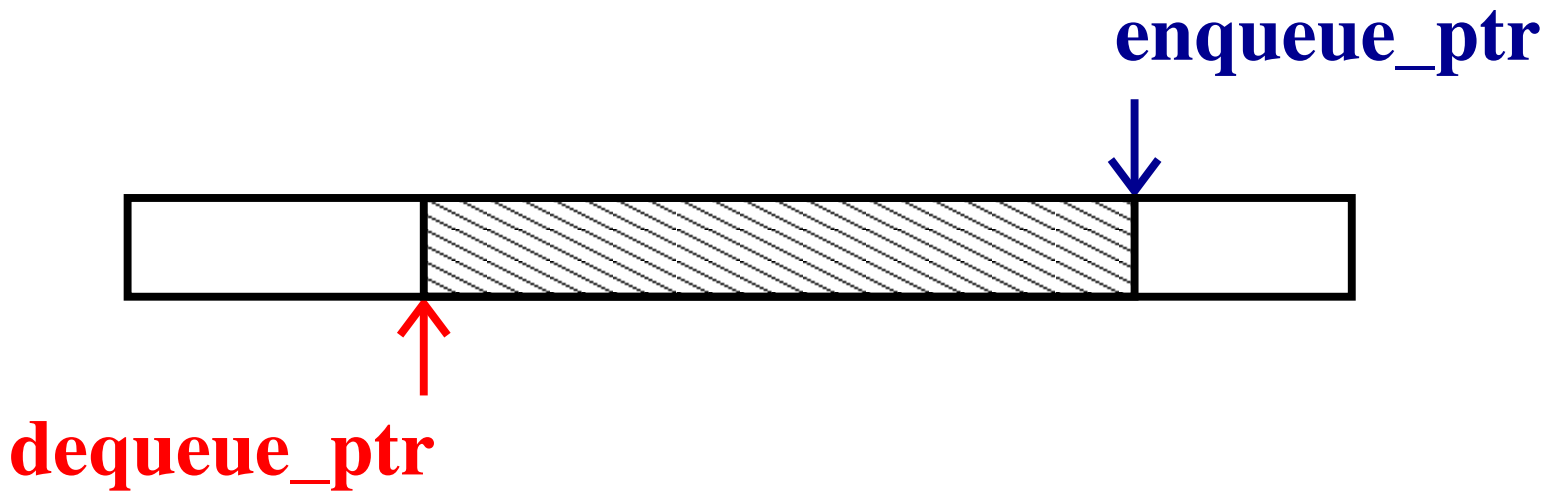
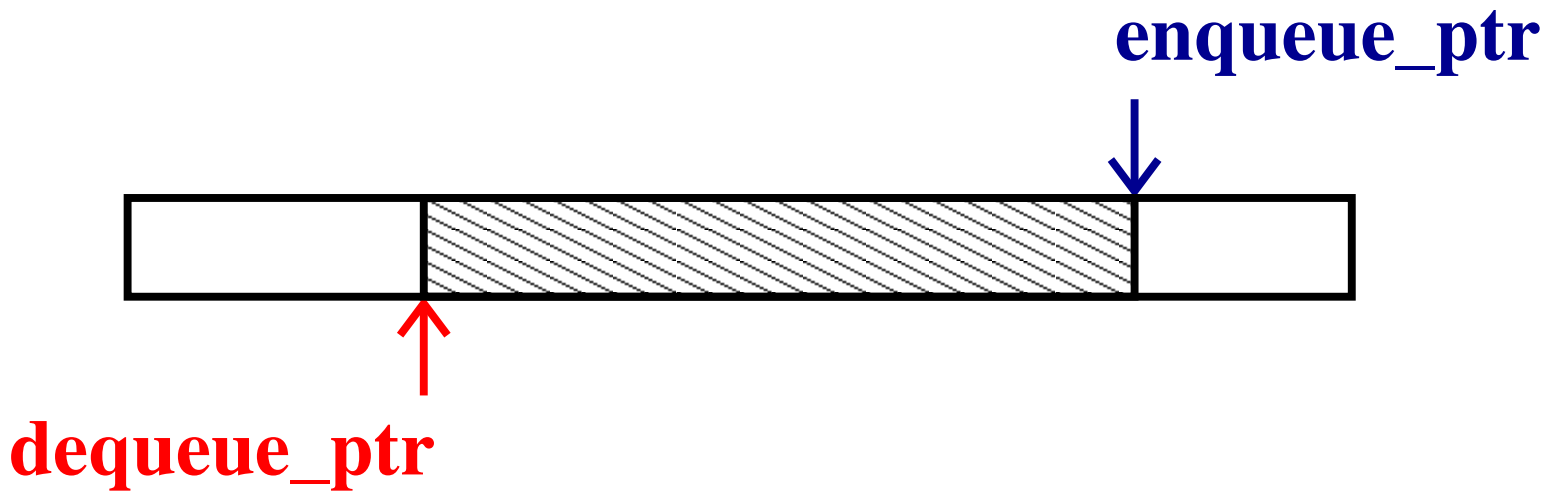
Lamport's Queue Bottlenecks



while(**next_enqueue_ptr** == **dequeue_ptr**){;}

Performance degradation due to:

Lamport's Queue Bottlenecks



while(**next_enqueue_ptr** == **dequeue_ptr**){;}

Performance degradation due to:

- Frequent thread synchronisation

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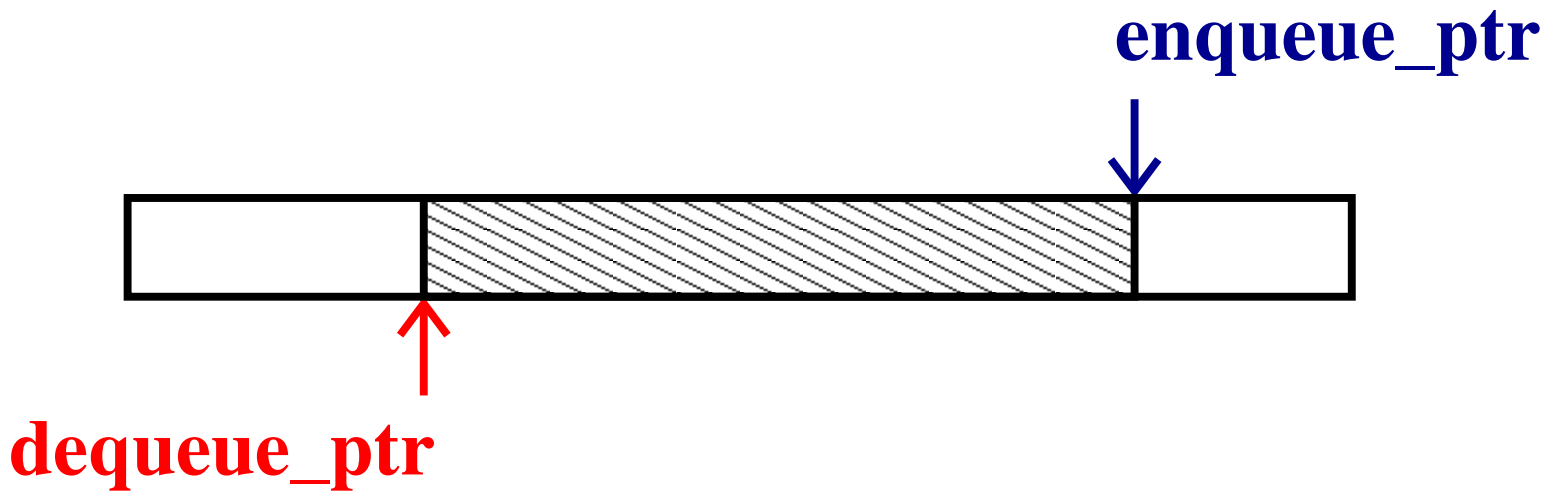

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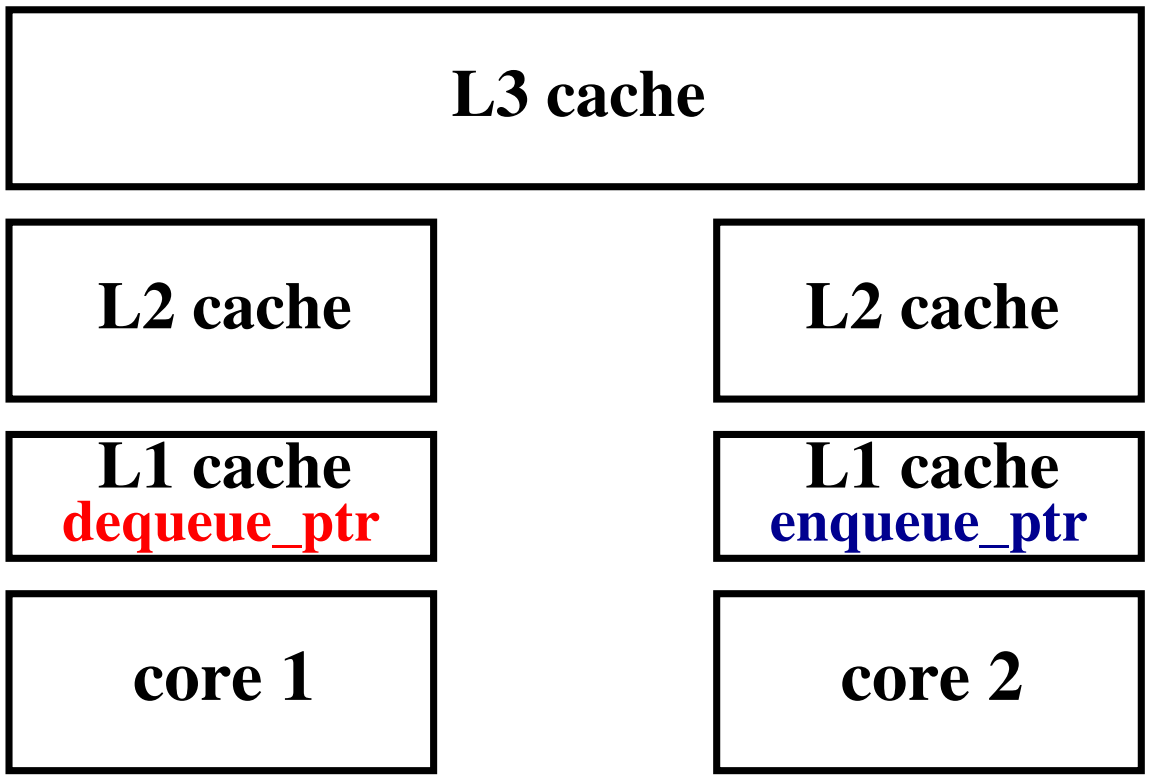
Performance degradation due to:

- Frequent thread synchronisation
- Cache ping-pong

Cache Ping-Pong

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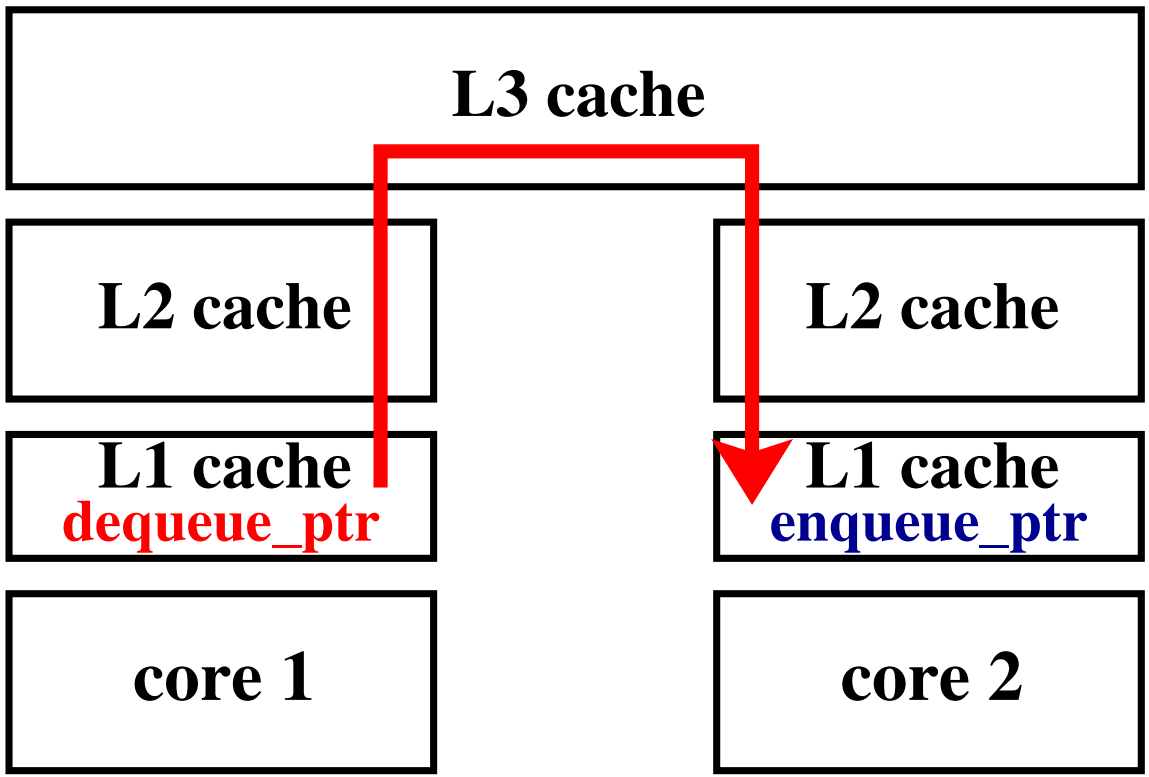
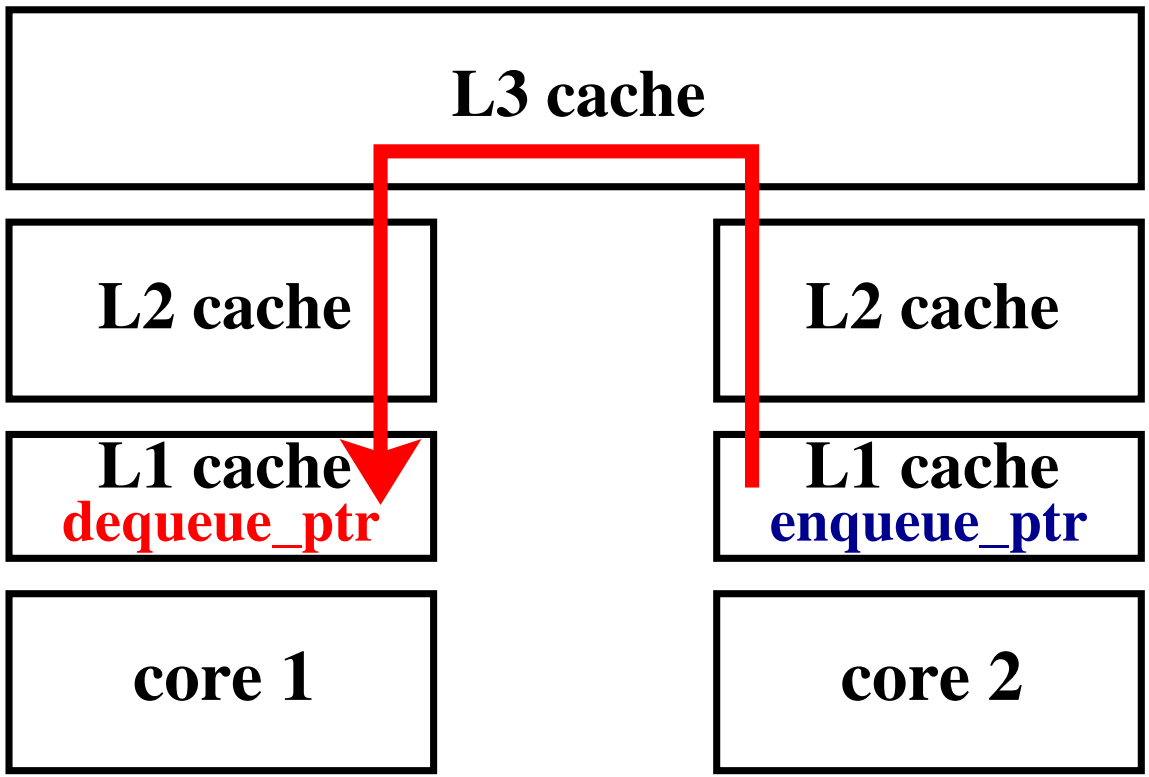
Cache Ping-Pong



while(**next_enqueue_ptr** == **dequeue_ptr**){;}

- Queue pointers ping-pong across cache hierarchy

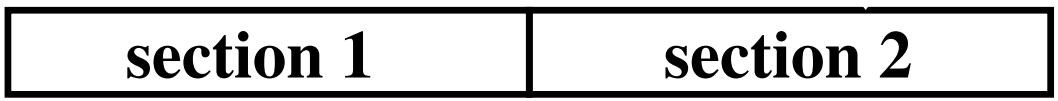
Cache Ping-Pong



while(**next_dequeue_ptr** == **enqueue_ptr**){;}

- Queue pointers ping-pong across cache hierarchy

Multi-Section Queue(MSQ): state-of-the-art



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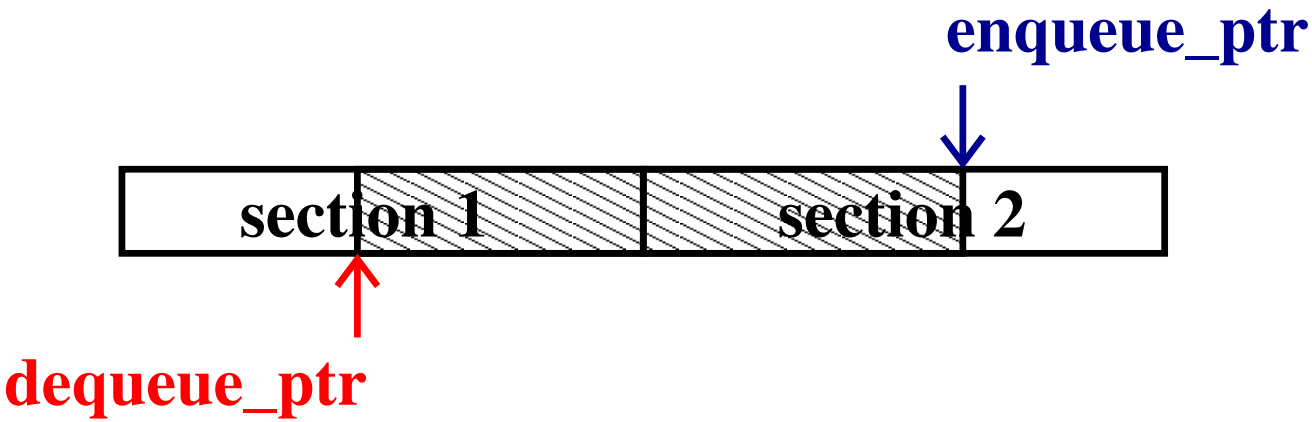
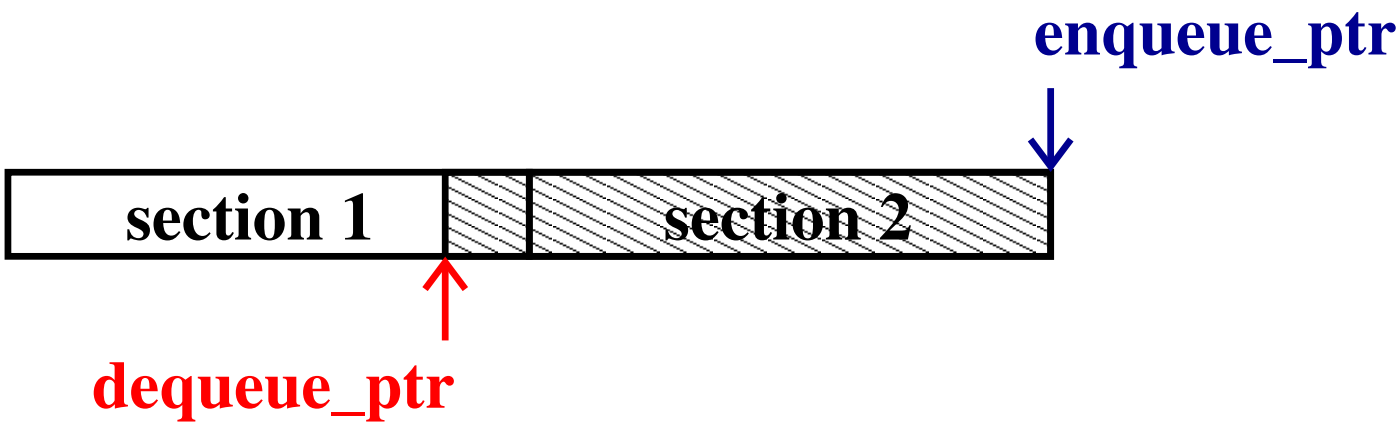


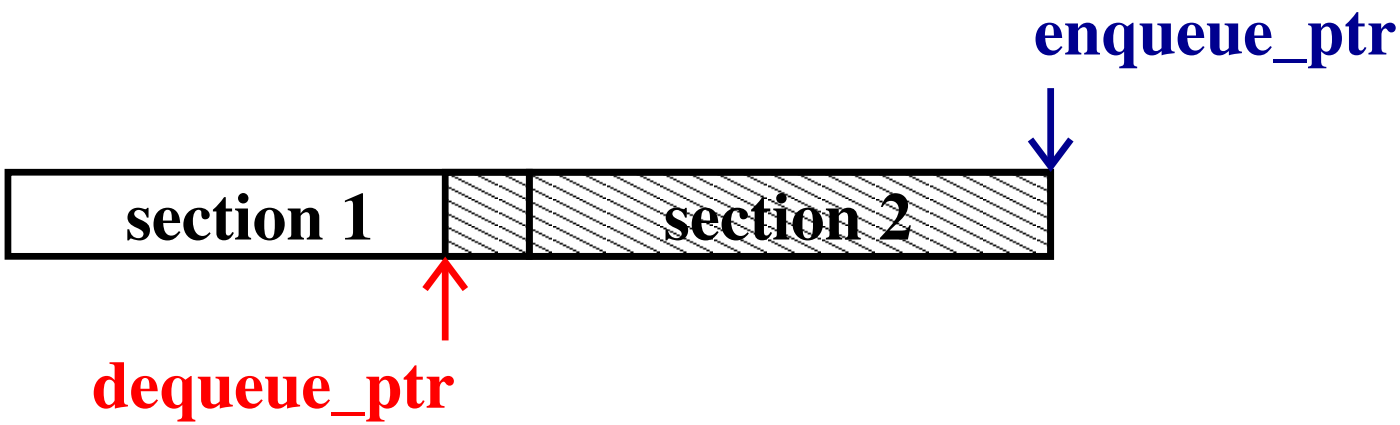
- Each section is exclusively used by one thread

Multi-Section Queue(MSQ): state-of-the-art



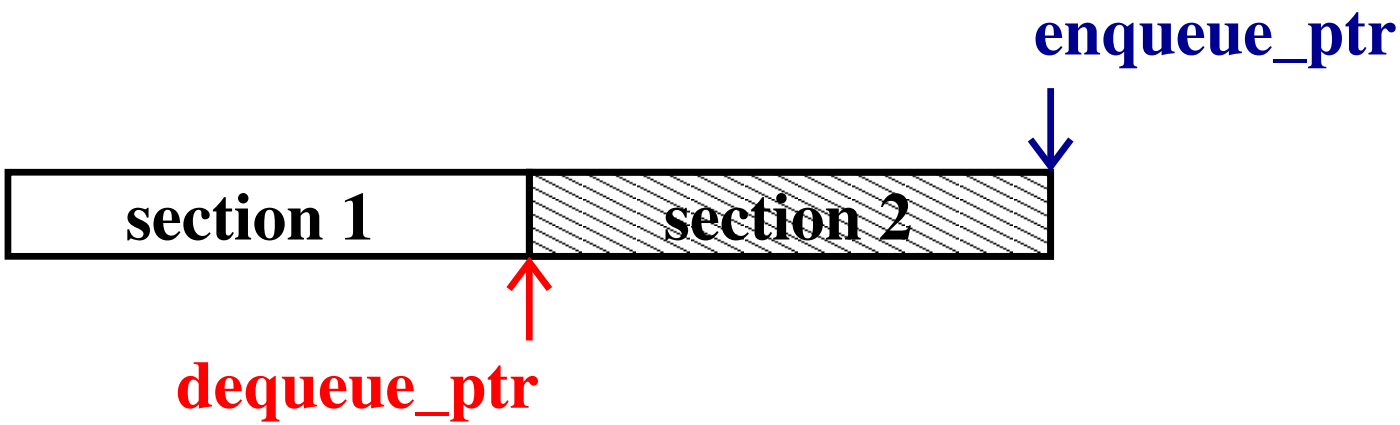
- Enqueue thread cannot access section 1 because dequeue thread still uses it

Multi-Section Queue(MSQ): state-of-the-art



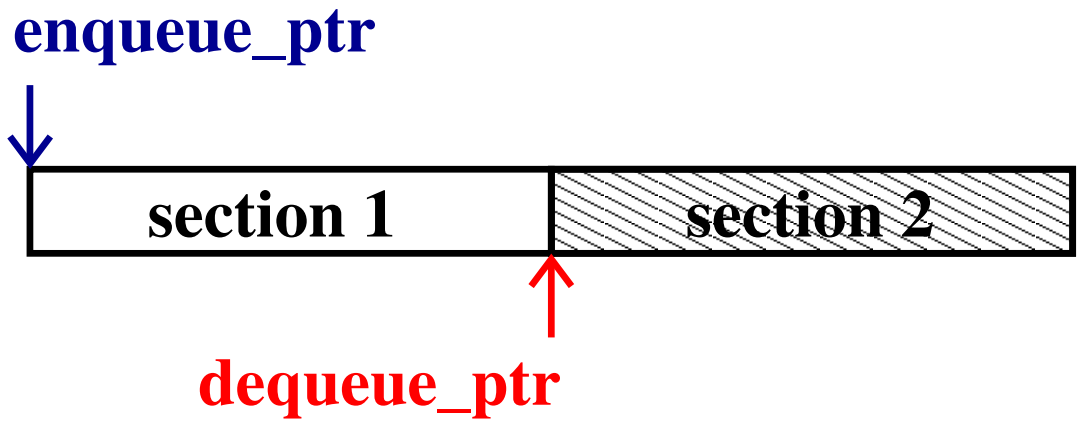
- Enqueue thread cannot access section 1 because dequeue thread still uses it
- Enqueue thread waits (spins) at the end of section 2

Multi-Section Queue(MSQ): state-of-the-art



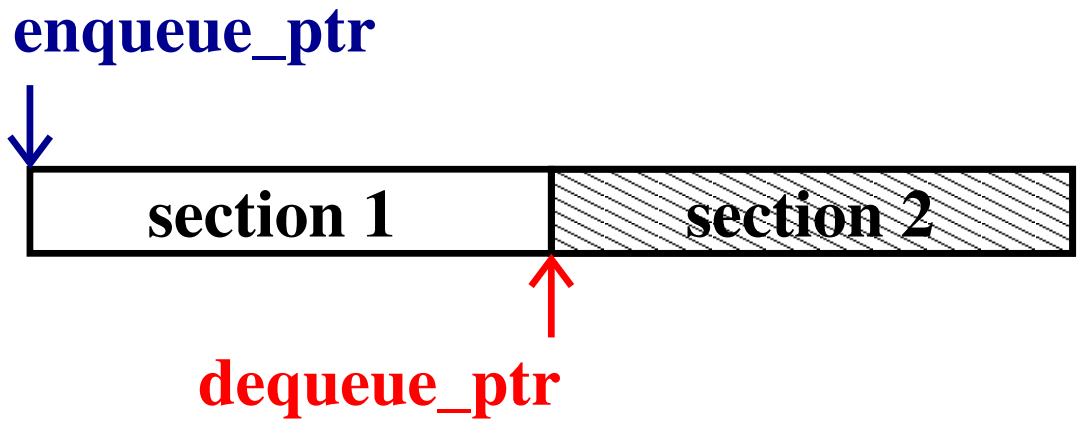
- Dequeue thread reached the end of section 1

Multi-Section Queue(MSQ): state-of-the-art



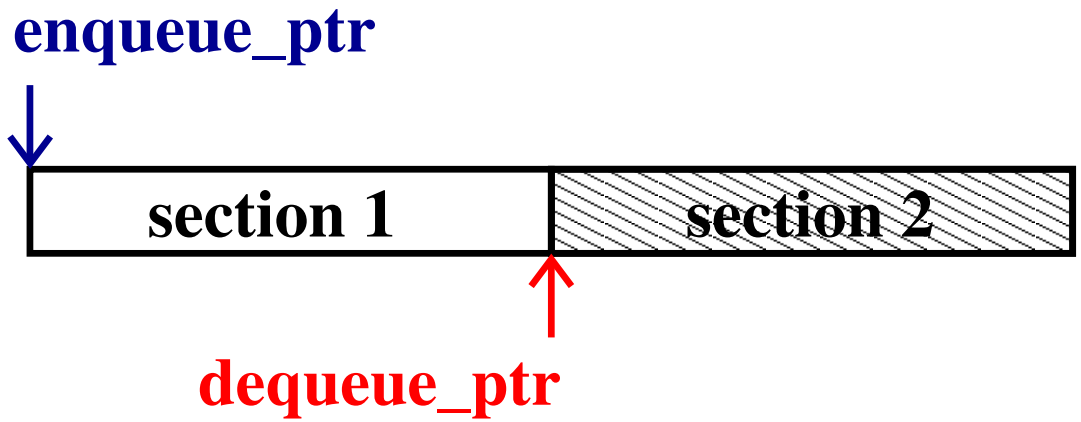
- Dequeue thread reached the end of section 1
- Enqueue thread enters section 1

Multi-Section Queue(MSQ): state-of-the-art



Performance optimisations:

Multi-Section Queue(MSQ): state-of-the-art



Performance optimisations:

- Infrequent boundary checks (less frequent synchronisation)

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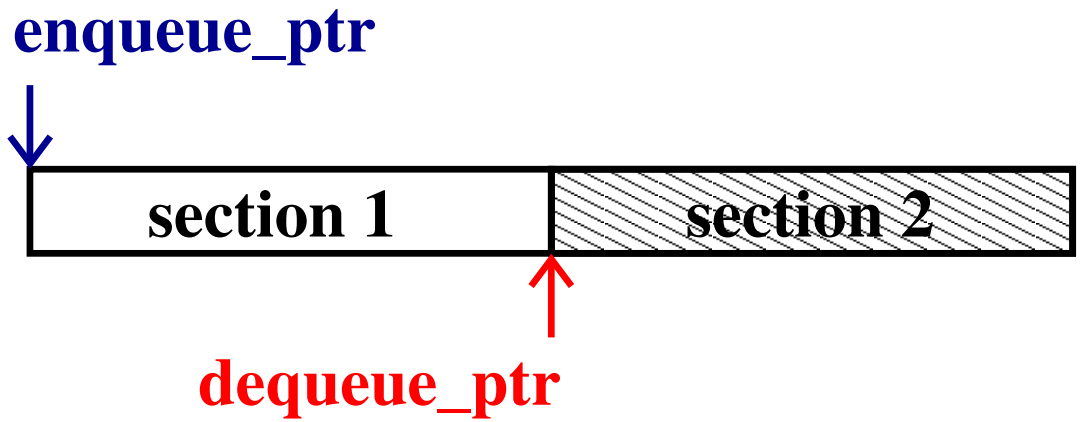
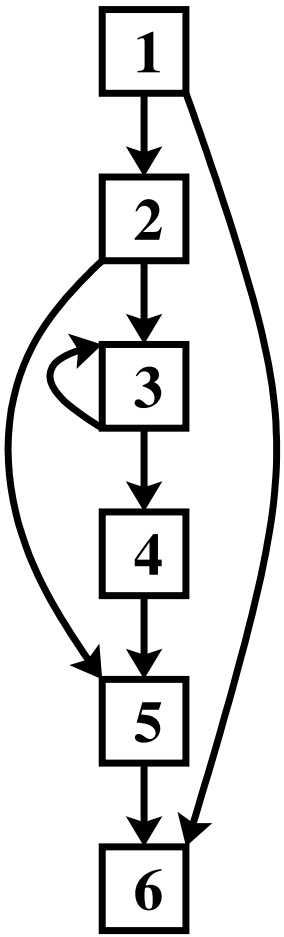


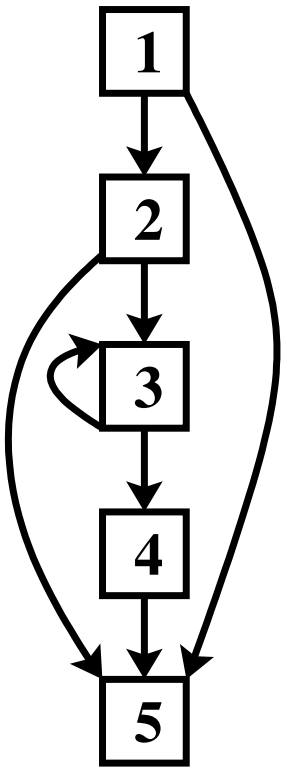
Performance optimisations:

- Infrequent boundary checks (less frequent synchronisation)
- Reduced cache ping-pong

MSQ Control-Flow Graph and Internals



enqueue function



dequeue function

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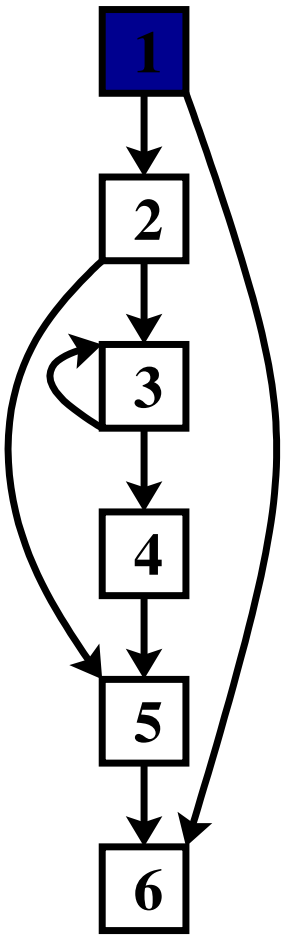

enqueue function

enqueue

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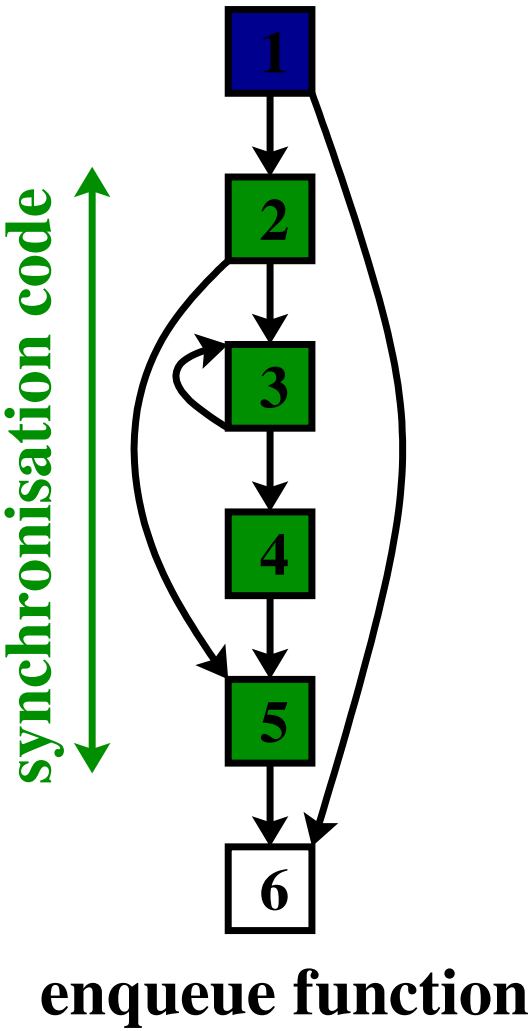

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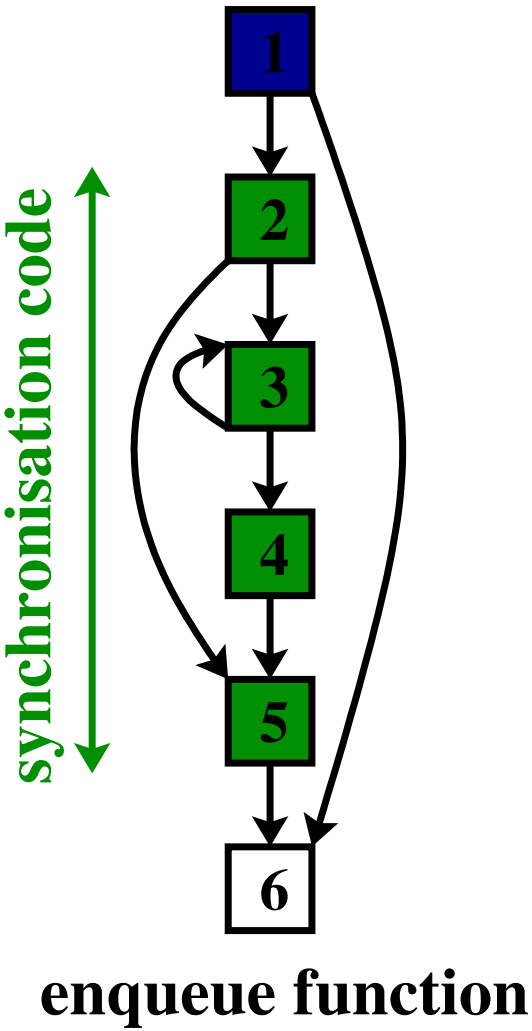

enqueue

checks if next section is free

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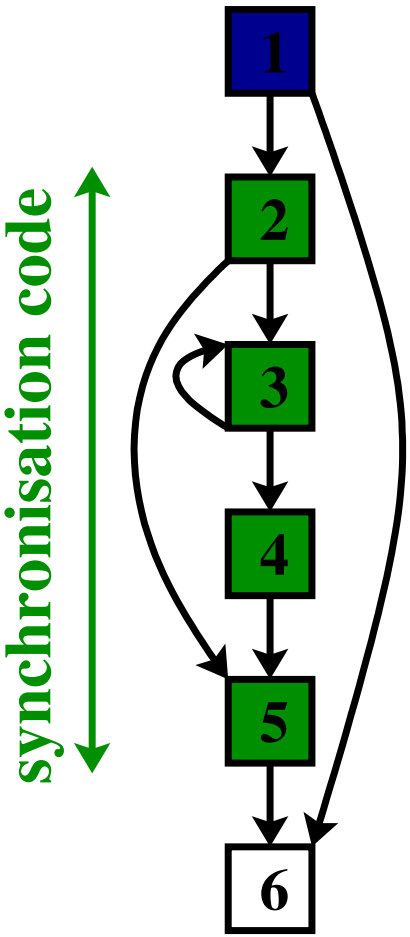


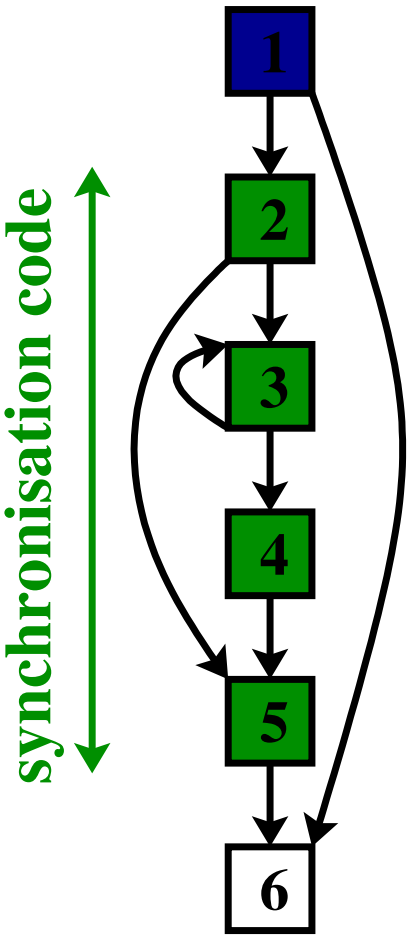
enqueue function

enqueue

checks if next section is free

spin loop

MSQ Control-Flow Graph and Internals



enqueue function

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update local variables

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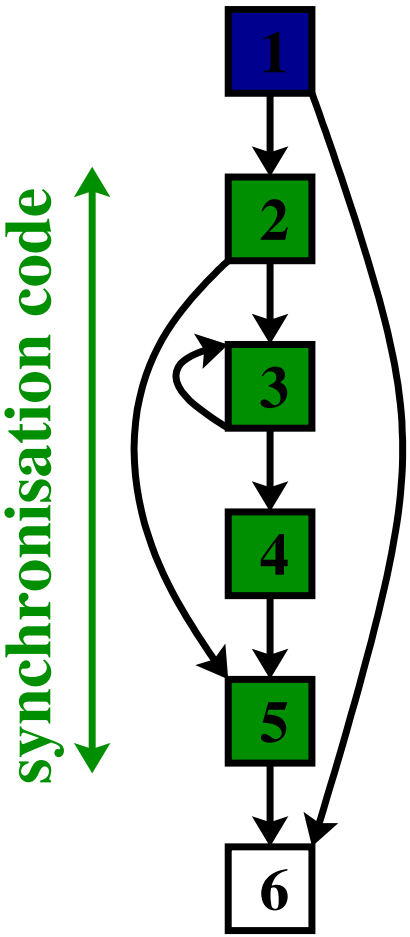

enqueue function

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checks if next section is free

spin loop

update local variables

update shared variable

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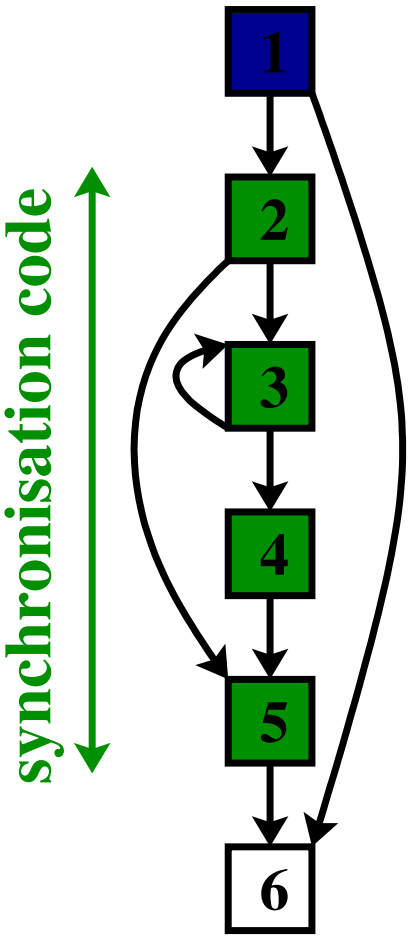

enqueue function

enqueue

checks if next section is free

spin loop

update local variables

update shared variable

join basic–block

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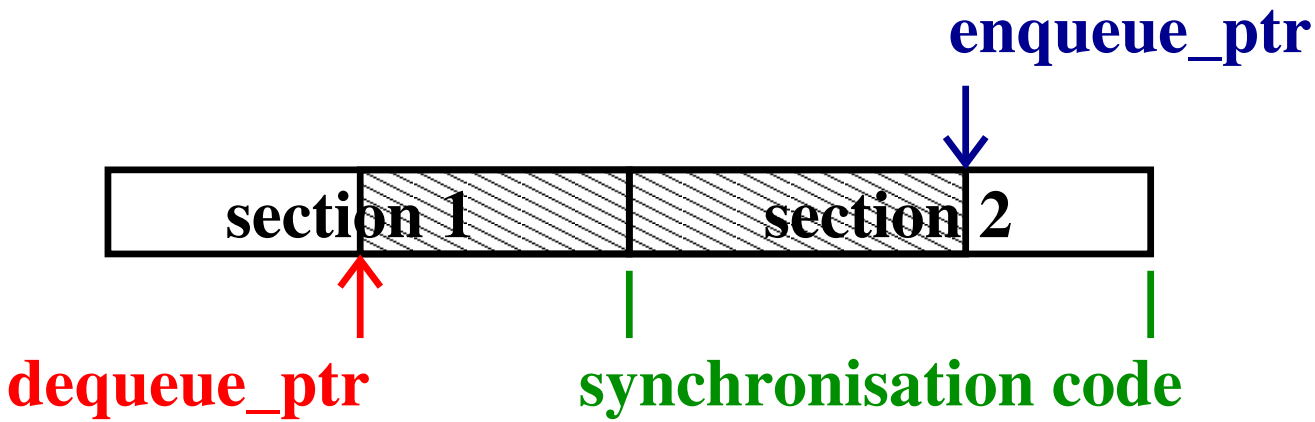

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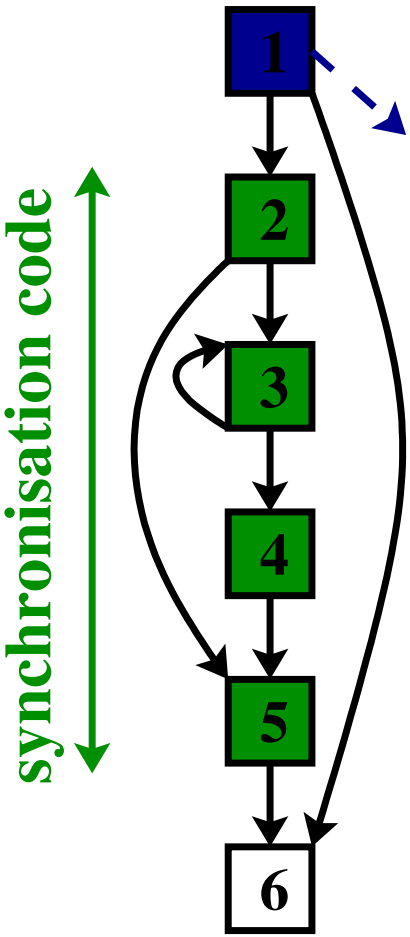

enqueue

```
lea rax, [rdx+8]

mov QWORD PTR [rdx], rcx

mov rdx, rax

and rdx, ROTATE MASK

test eax, SECTION_MASK

jne .L2
```

enqueue function

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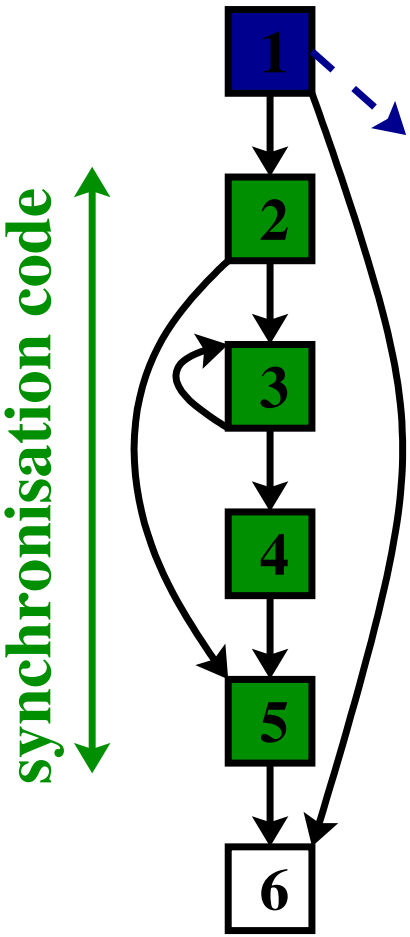

enqueue

```
lea rax, [rdx+8]                    incr pointer
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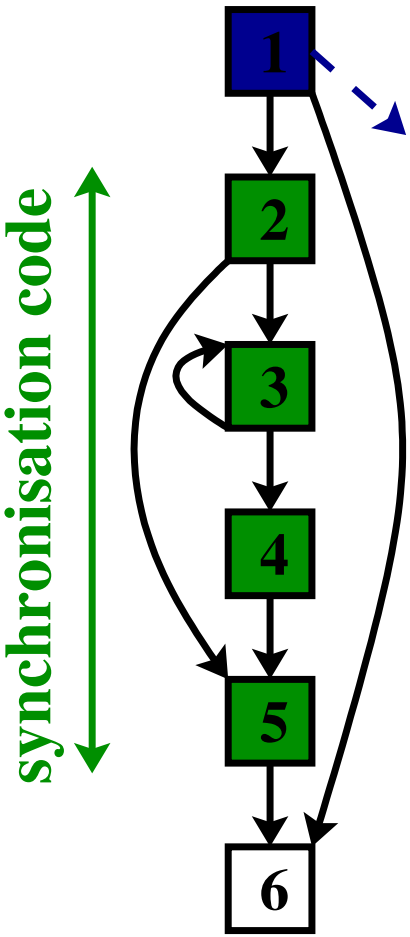

enqueue

```
lea rax, [rdx+8]                    incr pointer
mov QWORD PTR [rdx], rcx            store
mov rdx, rax
and rdx, ROTATE MASK
test eax, SECTION_MASK
jne .L2
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enqueue function

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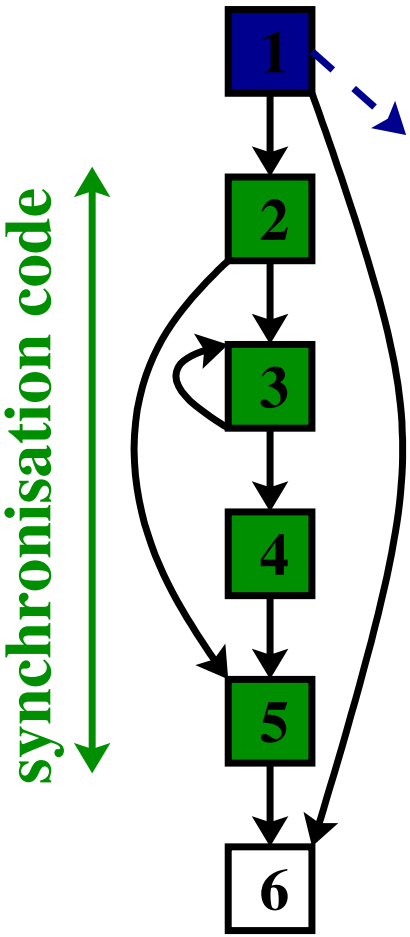

enqueue function

enqueue

lea rax, [rdx+8]	**incr pointer**
mov QWORD PTR [rdx], rcx	**store**
mov rdx, rax	**compiler's copy**
and rdx, ROTATE MASK	
test eax, SECTION_MASK	
jne .L2	

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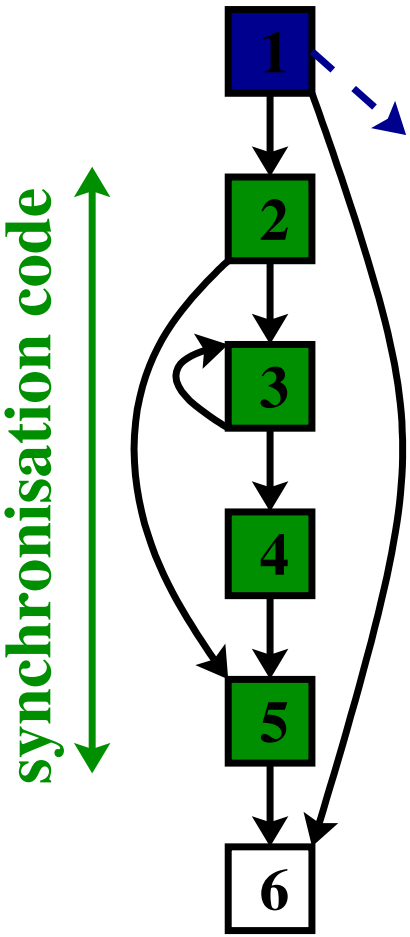

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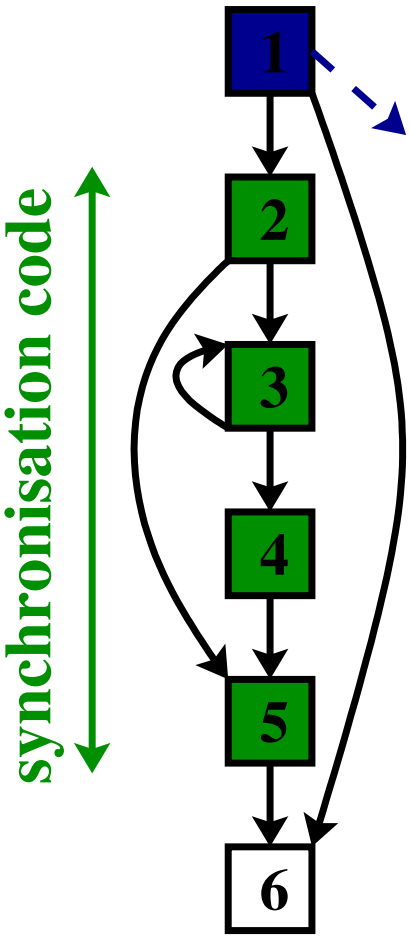
lea rax, [rdx+8]	**incr pointer**
mov QWORD PTR [rdx], rcx	**store**
mov rdx, rax	**compiler's copy**
and rdx, ROTATE MASK	**rotate pointer**
test eax, SECTION_MASK	
jne .L2	

MSQ Control-Flow Graph and Internals



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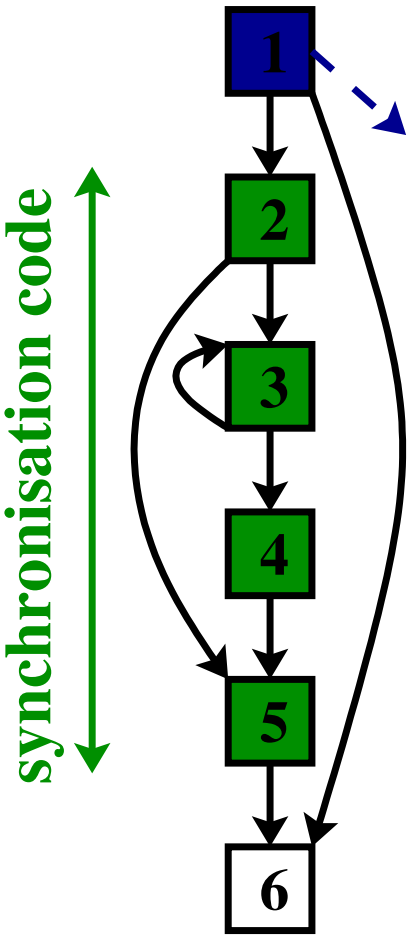

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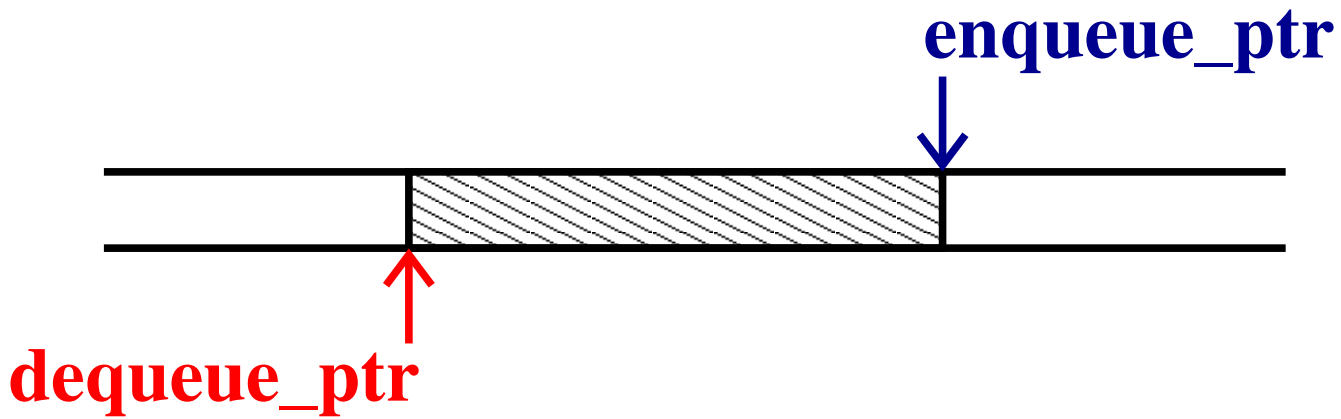
mov QWORD PTR [rdx], rcx	**store**
mov rdx, rax	**compiler's copy**
and rdx, ROTATE MASK	**rotate pointer**
test eax, SECTION_MASK	**end of section**
jne .L2	**skip sync code**

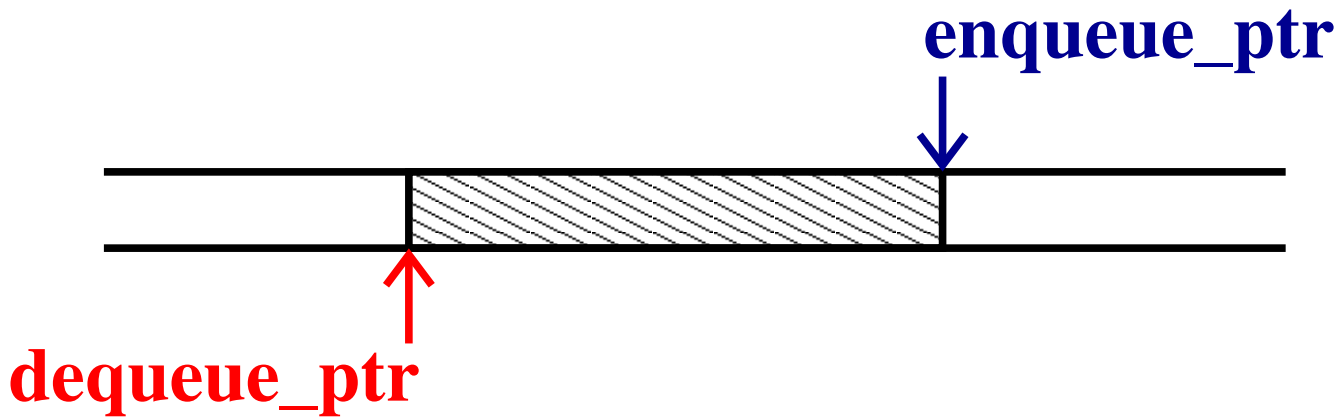
Optimal Queue



Optimal queue features:

- infinite size

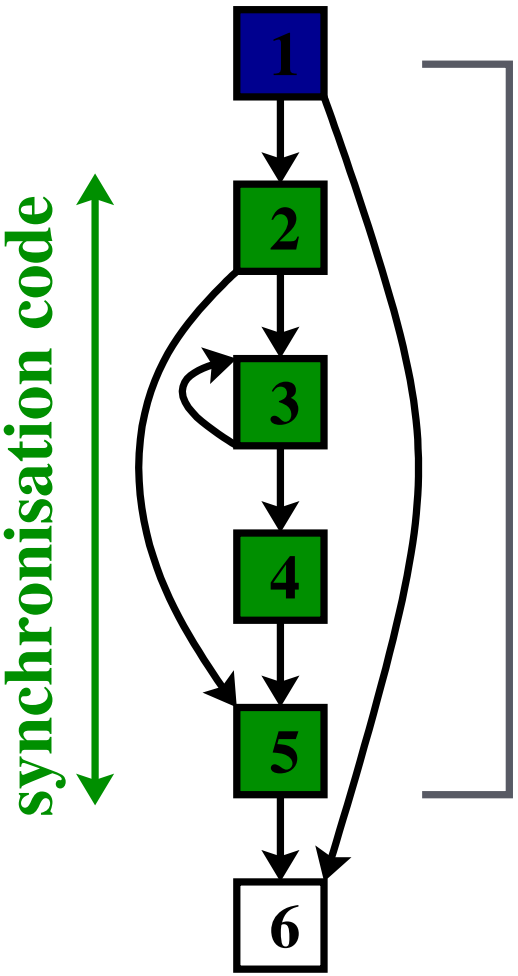
Optimal Queue



Optimal queue features:

- infinite size
- 2 instructions overhead
  1. pointer increment
  2. store into the queue

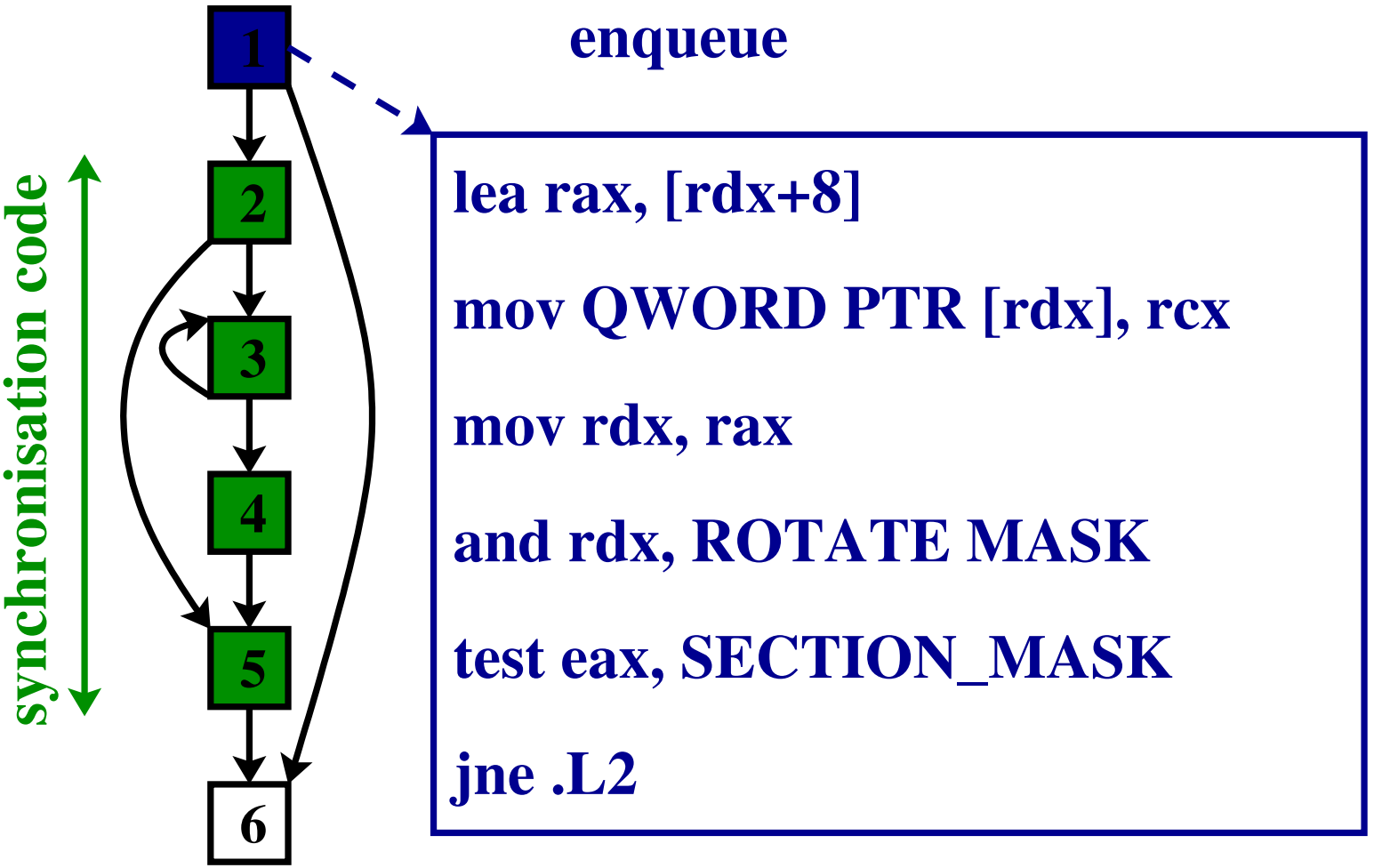
Lynx: Just 2 instructions overhead



enqueue function

Lynx removes part of enqueue (boundary checks) and all the synchronisation overhead off the critical path

Lynx(1): H/W triggered Synchronisation



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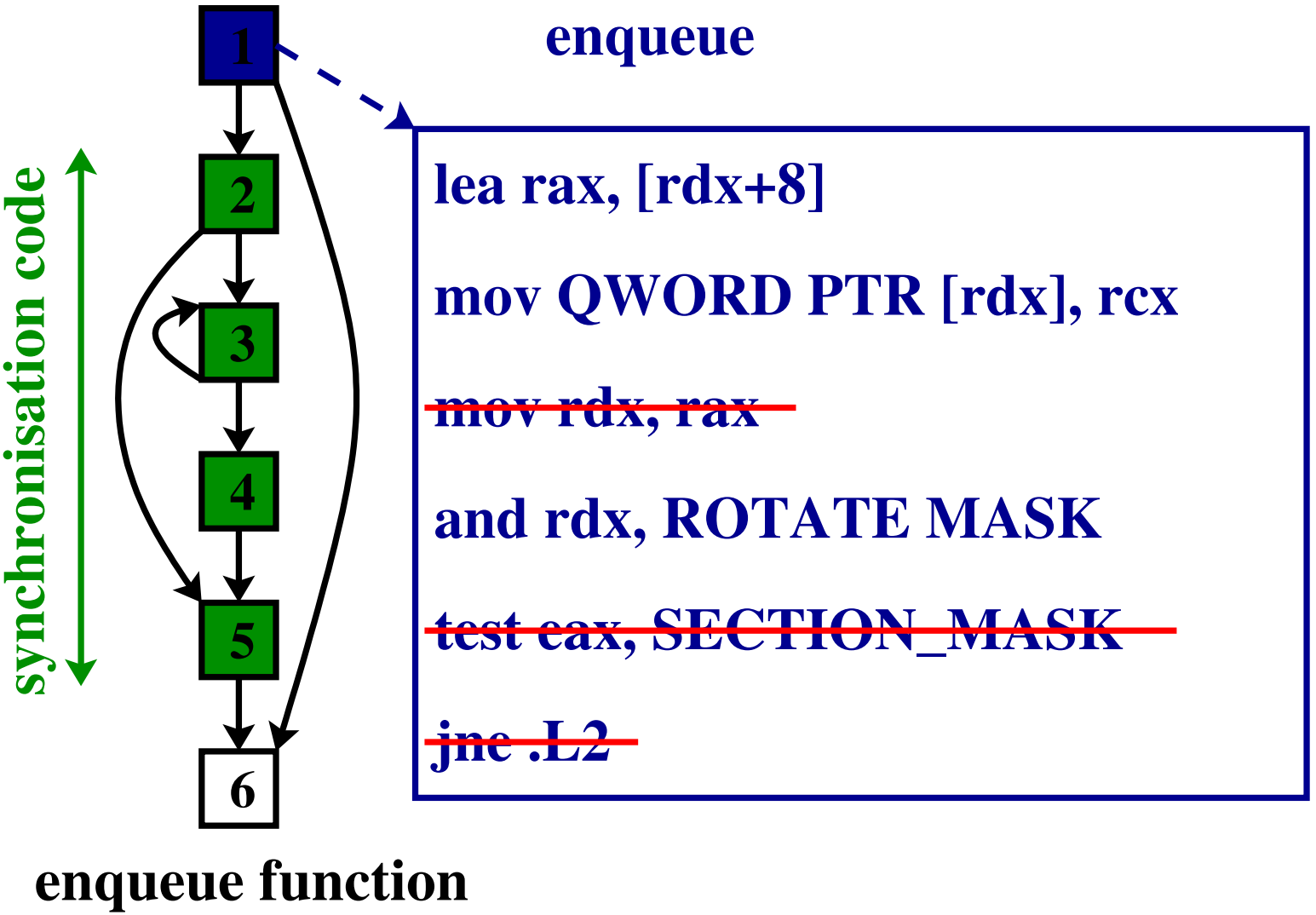

enqueue function

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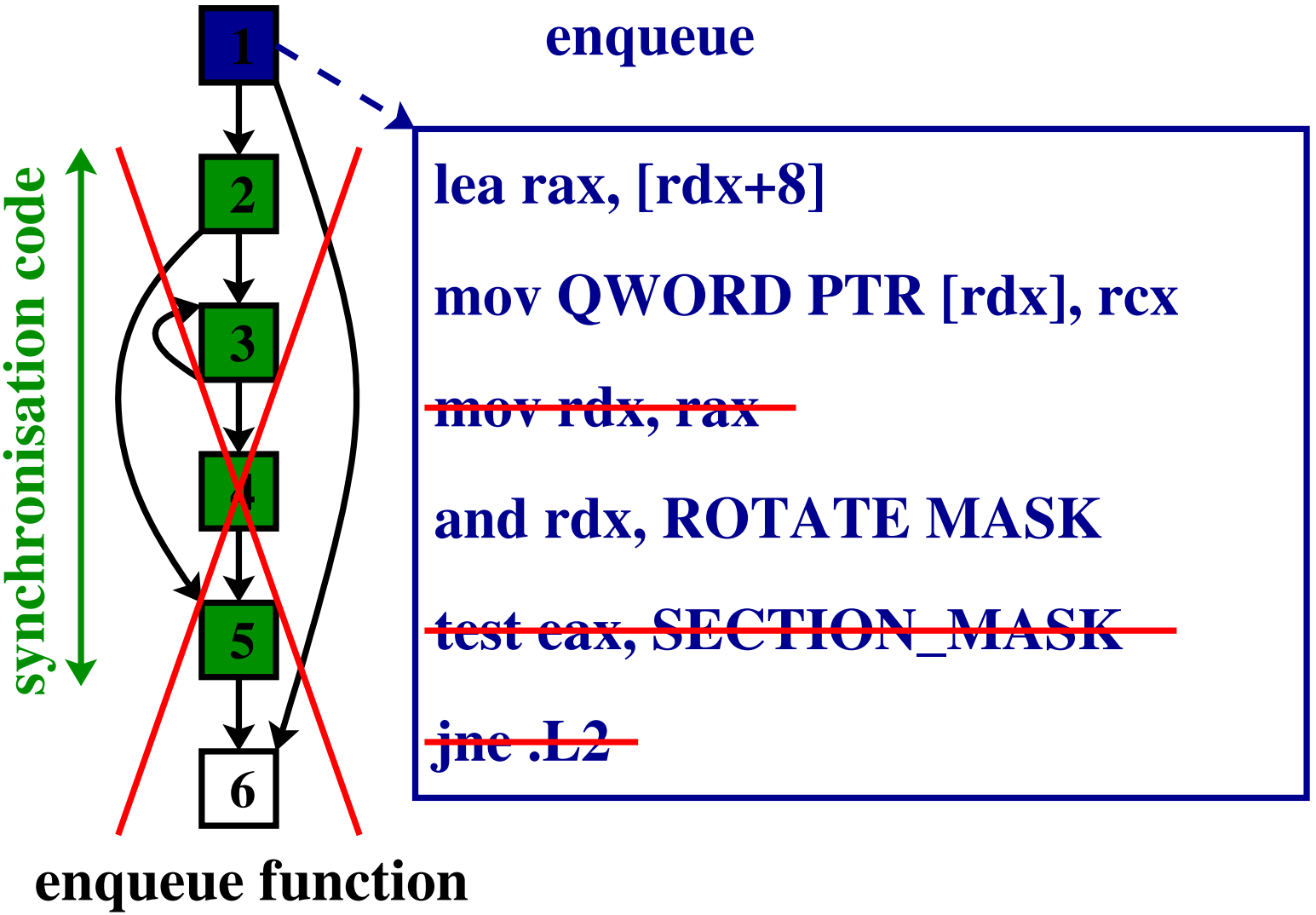

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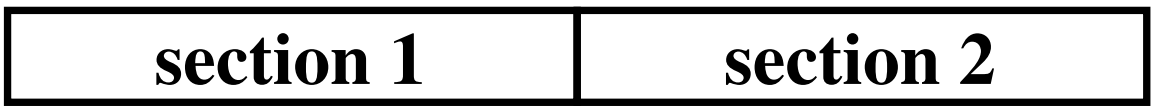

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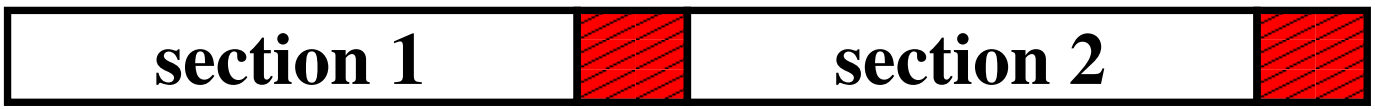
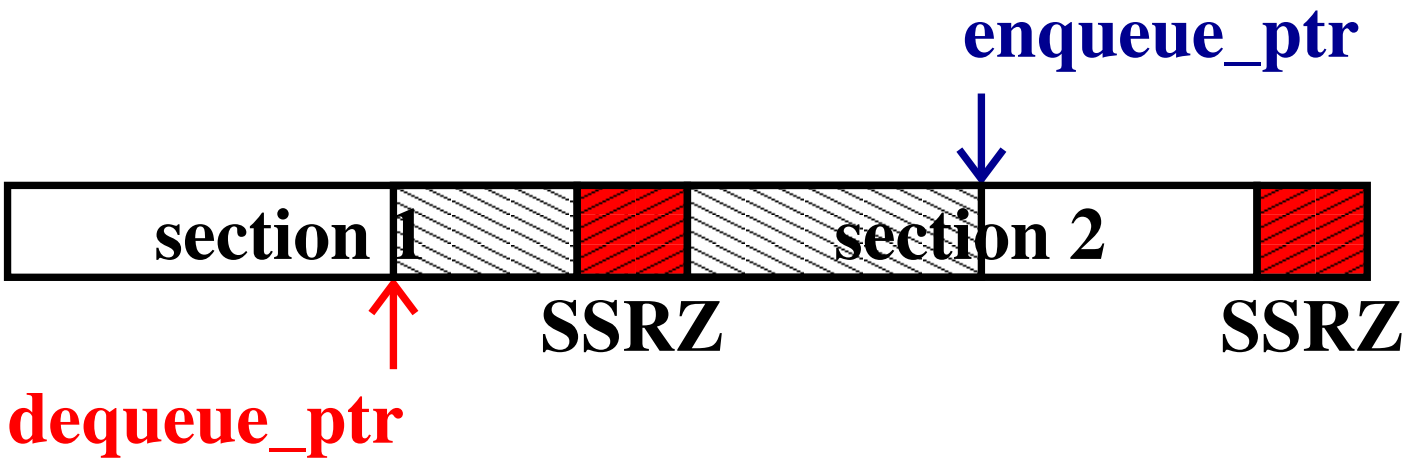


- A red zone is a non-read and non-write part of memory

Lynx(1): H/W triggered Synchronisation

- SSRZ: Section Synchronisation Red-Zone

Lynx(1): H/W triggered Synchronisation



Lynx(1): H/W triggered Synchronisation

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Lynx's handler checks:

- whether the SIG_SEGV is from the queue or the system
- which thread raised the exception
- if the thread is in section 1 or 2
- if the next section is free

Lynx(1): H/W triggered Synchronisation

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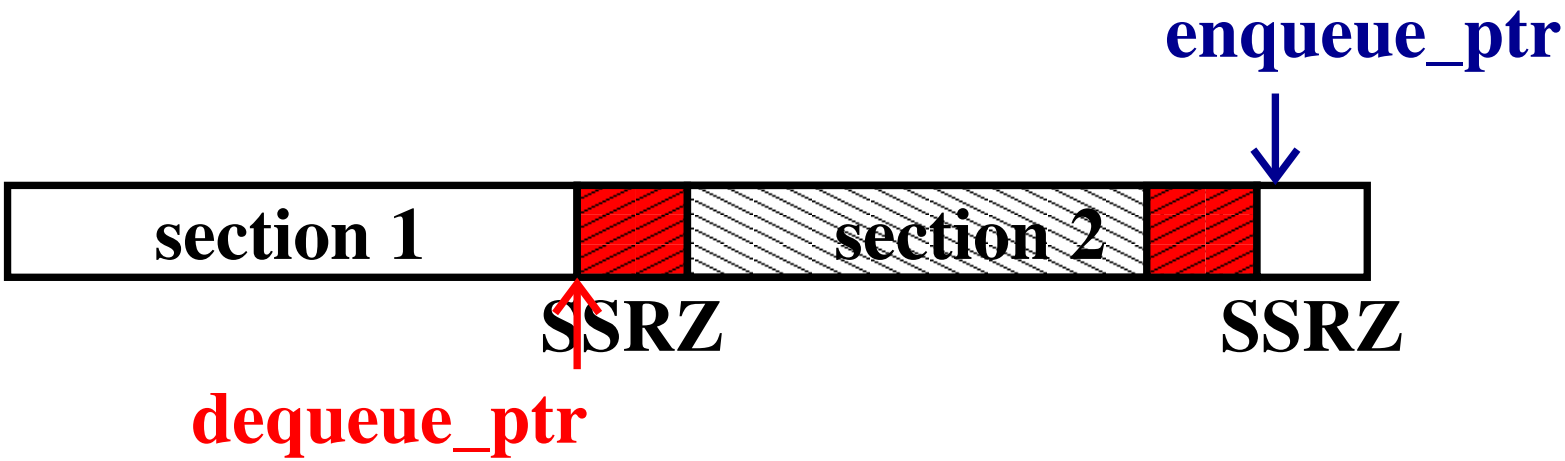
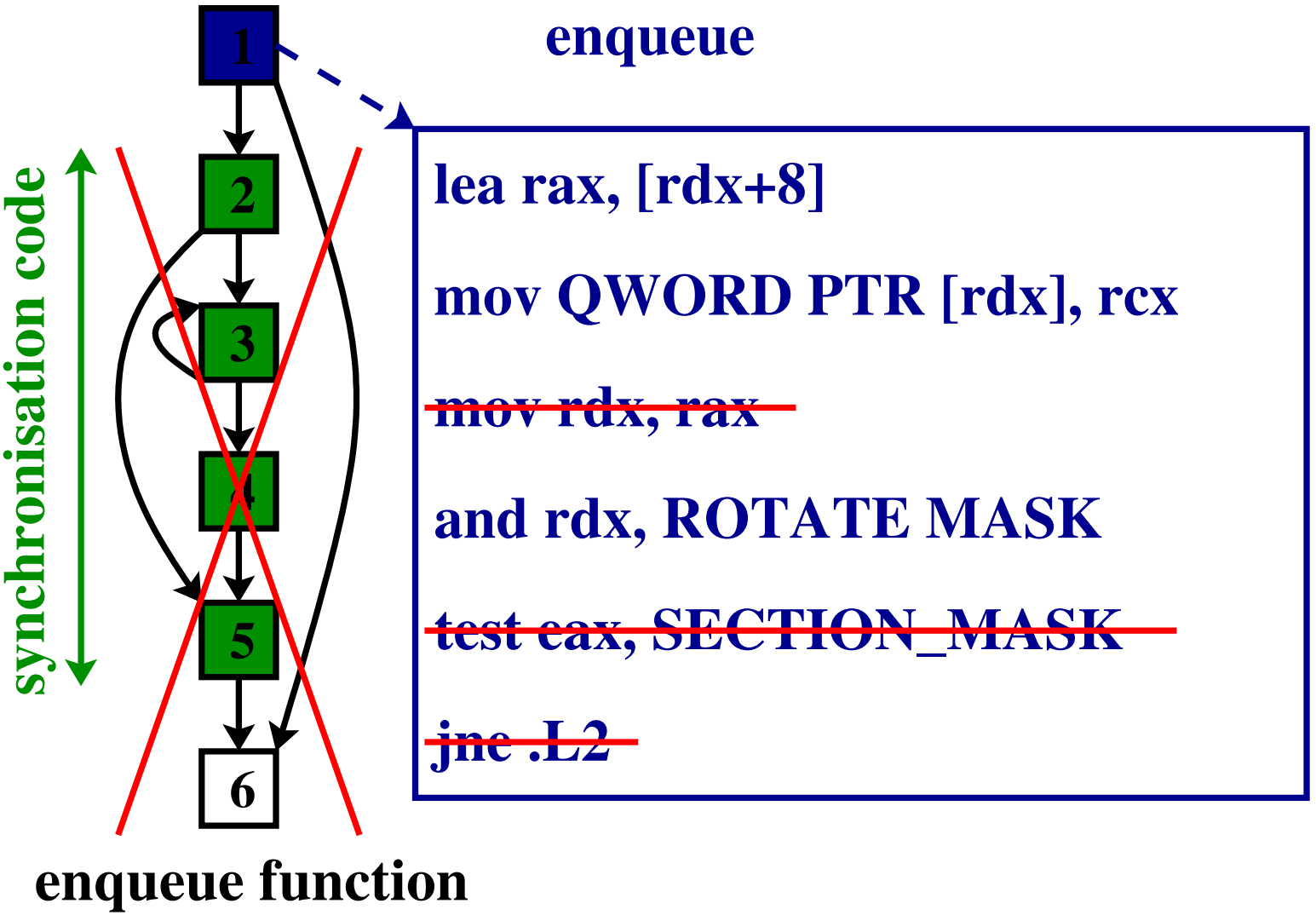


Lynx(2): H/W triggered Pointer Rotation



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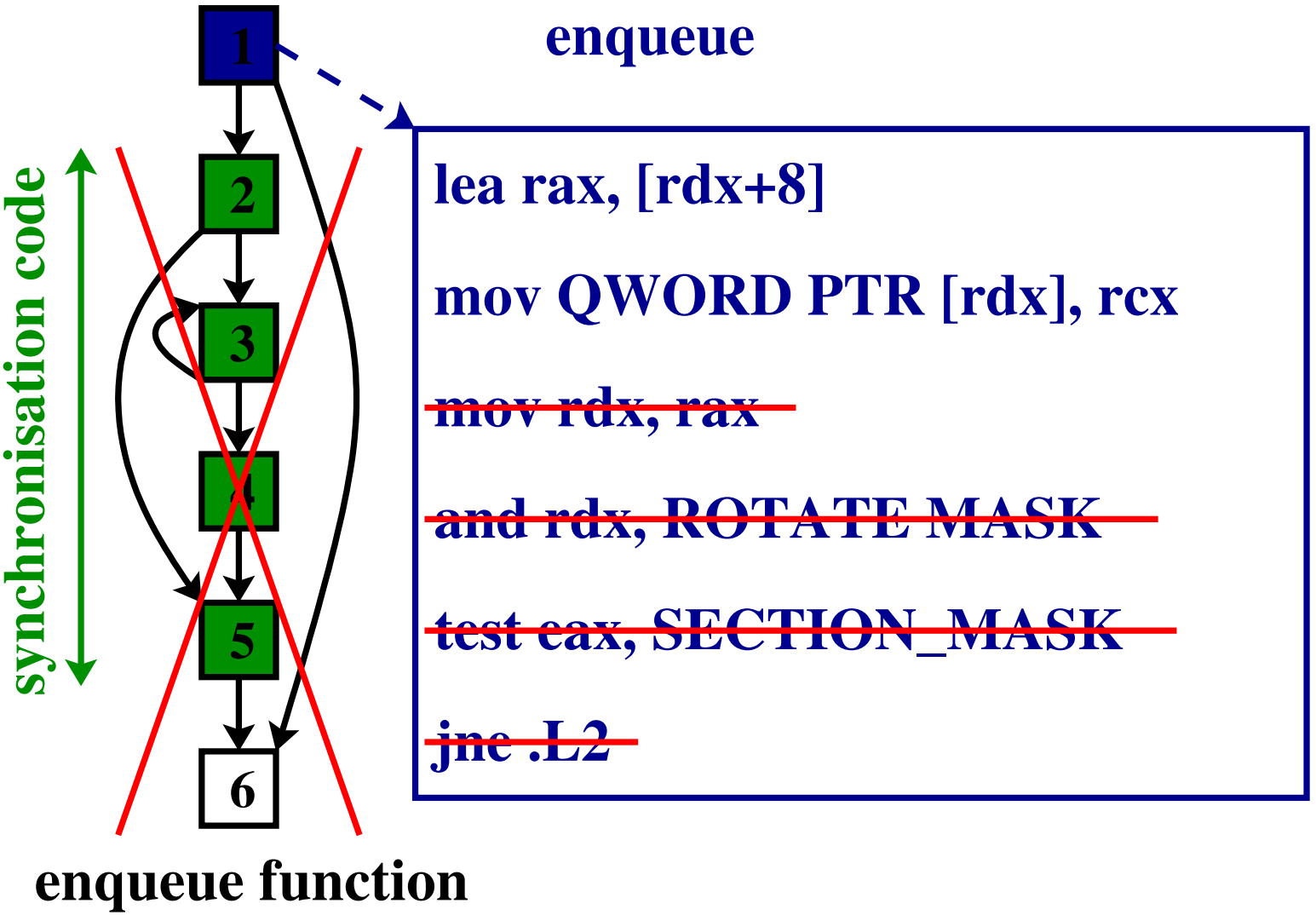
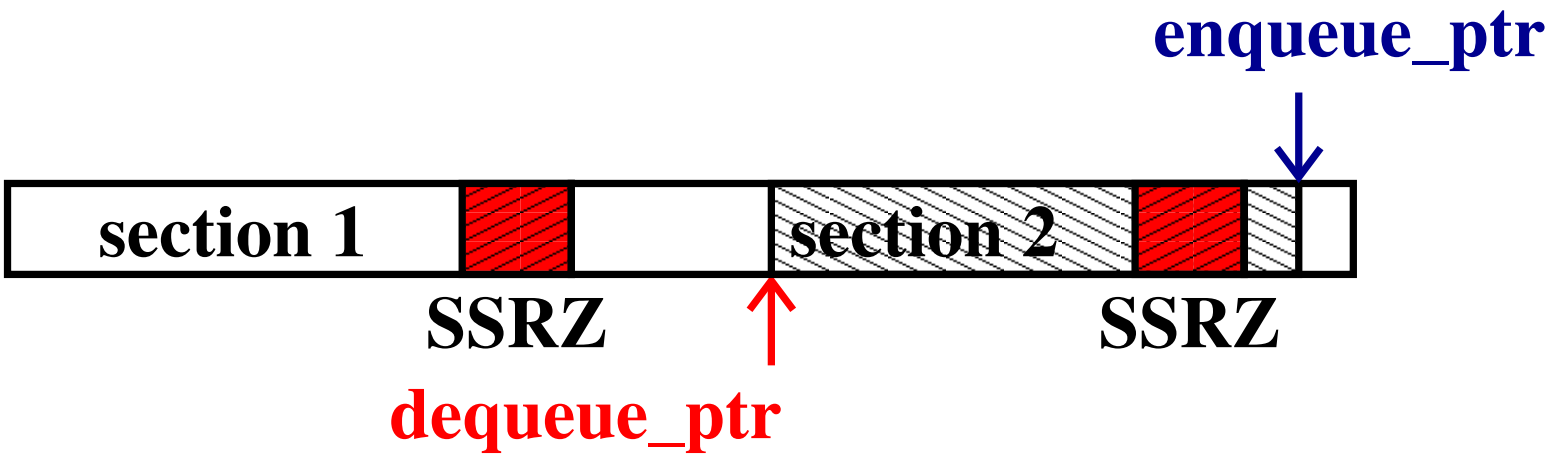


Lynx(2): H/W triggered Pointer Rotation



- SSRZ: Section Synchronisation Red-Zone

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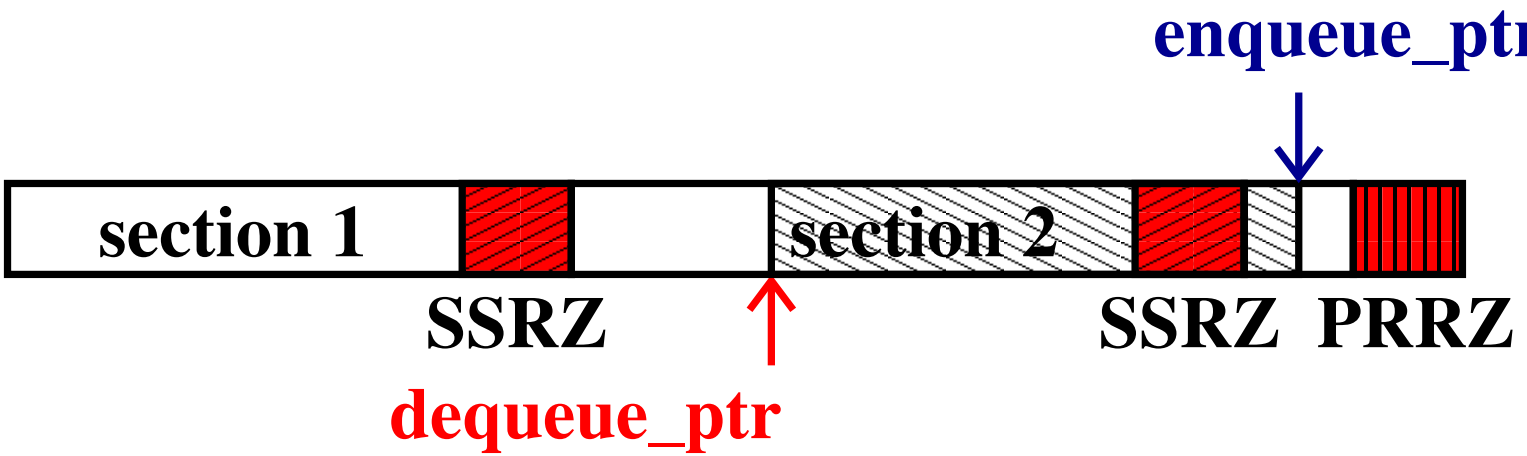

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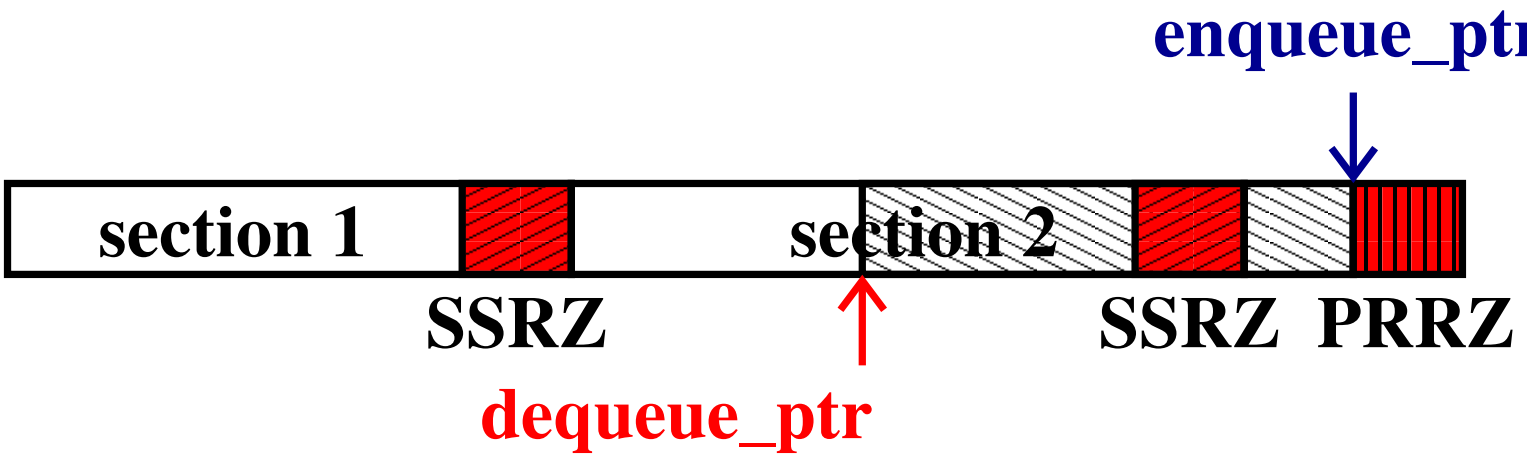

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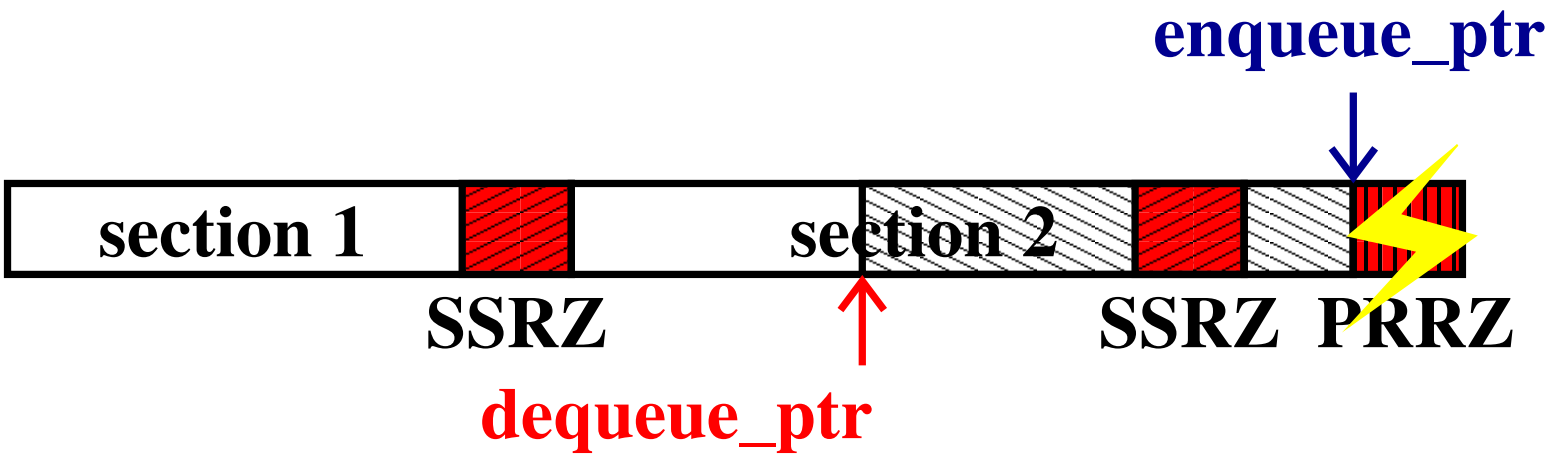

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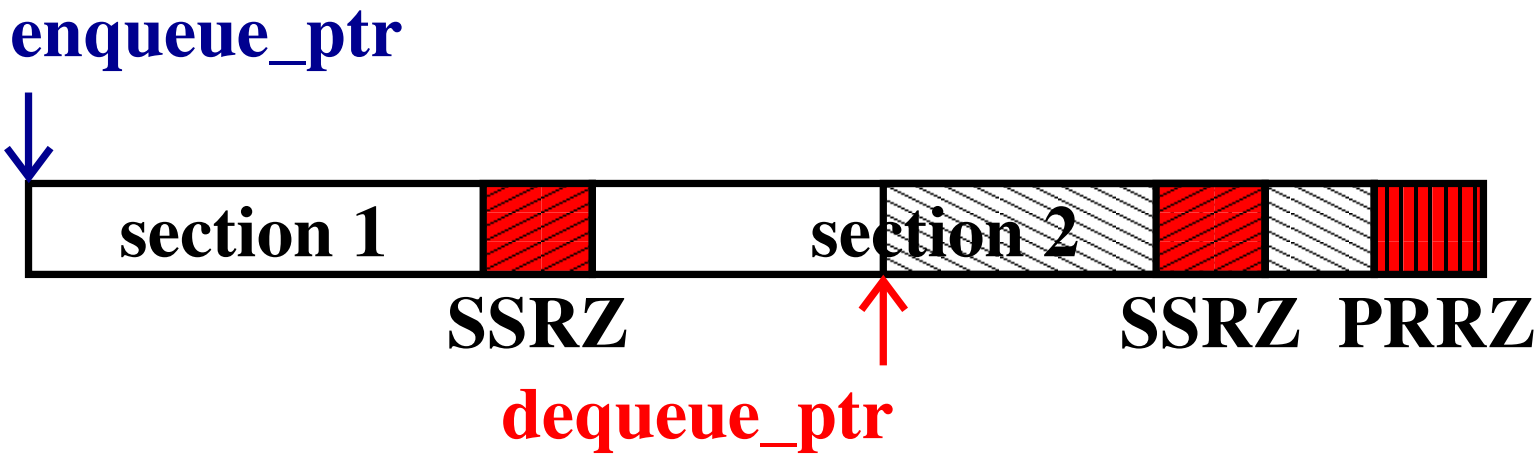

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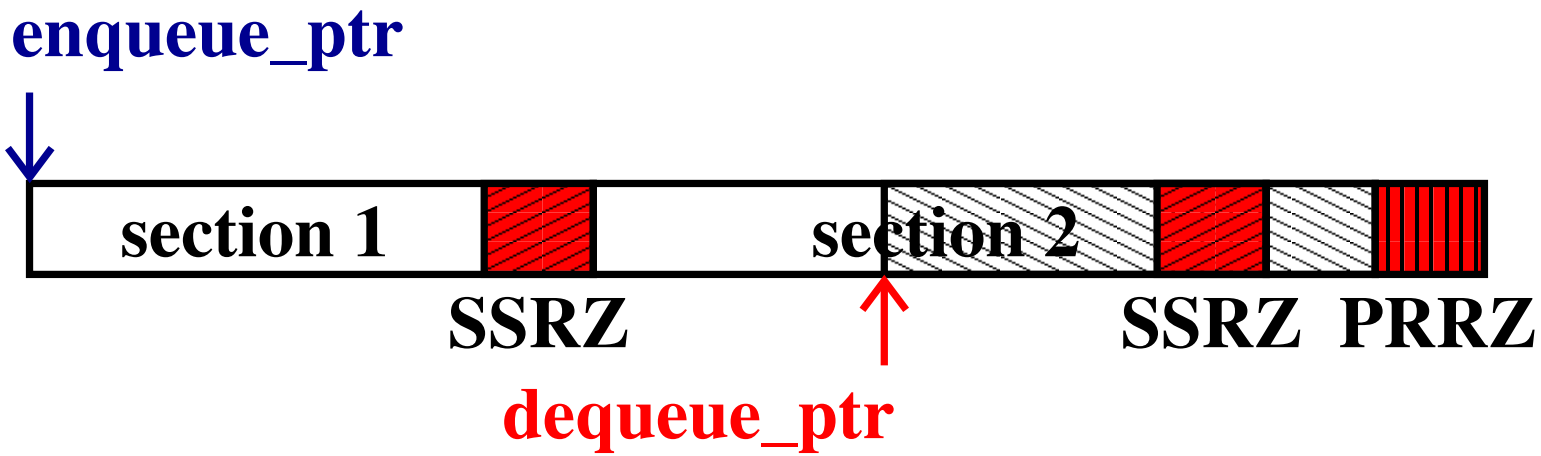
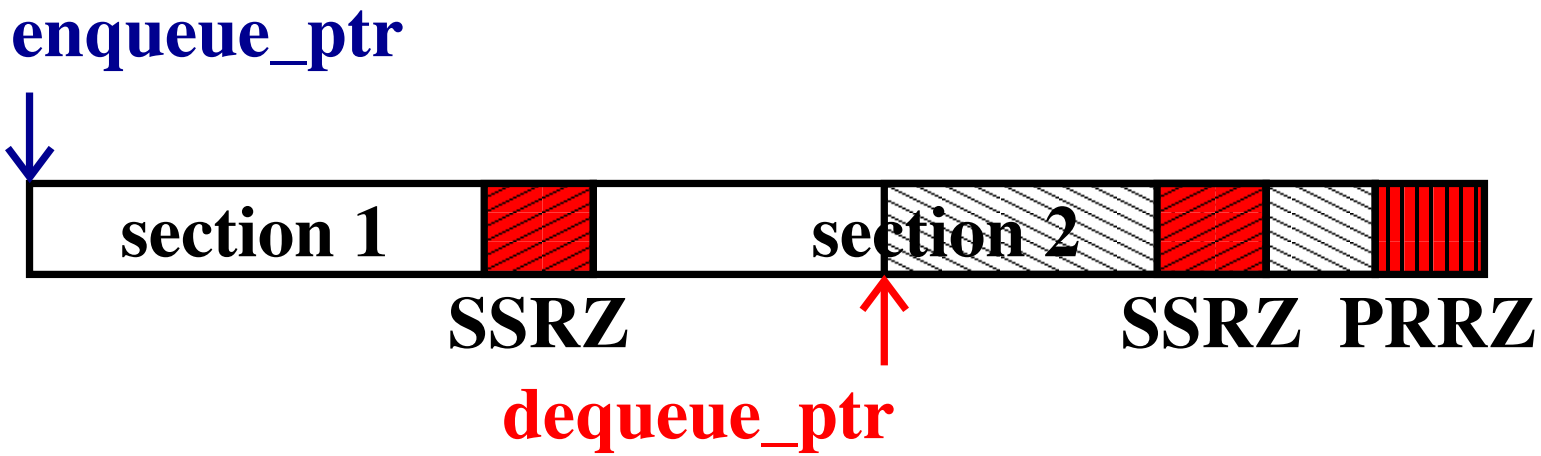


Two types of red-zones:

Lynx(2): H/W triggered Pointer Rotation



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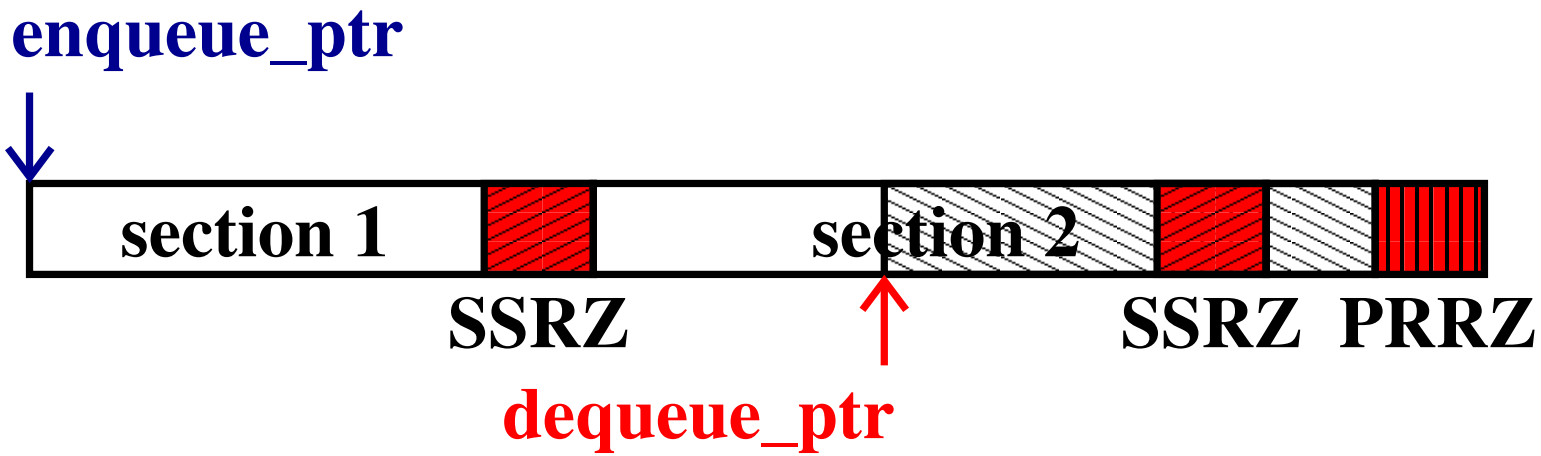

Two types of red-zones:

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Experimental Setup

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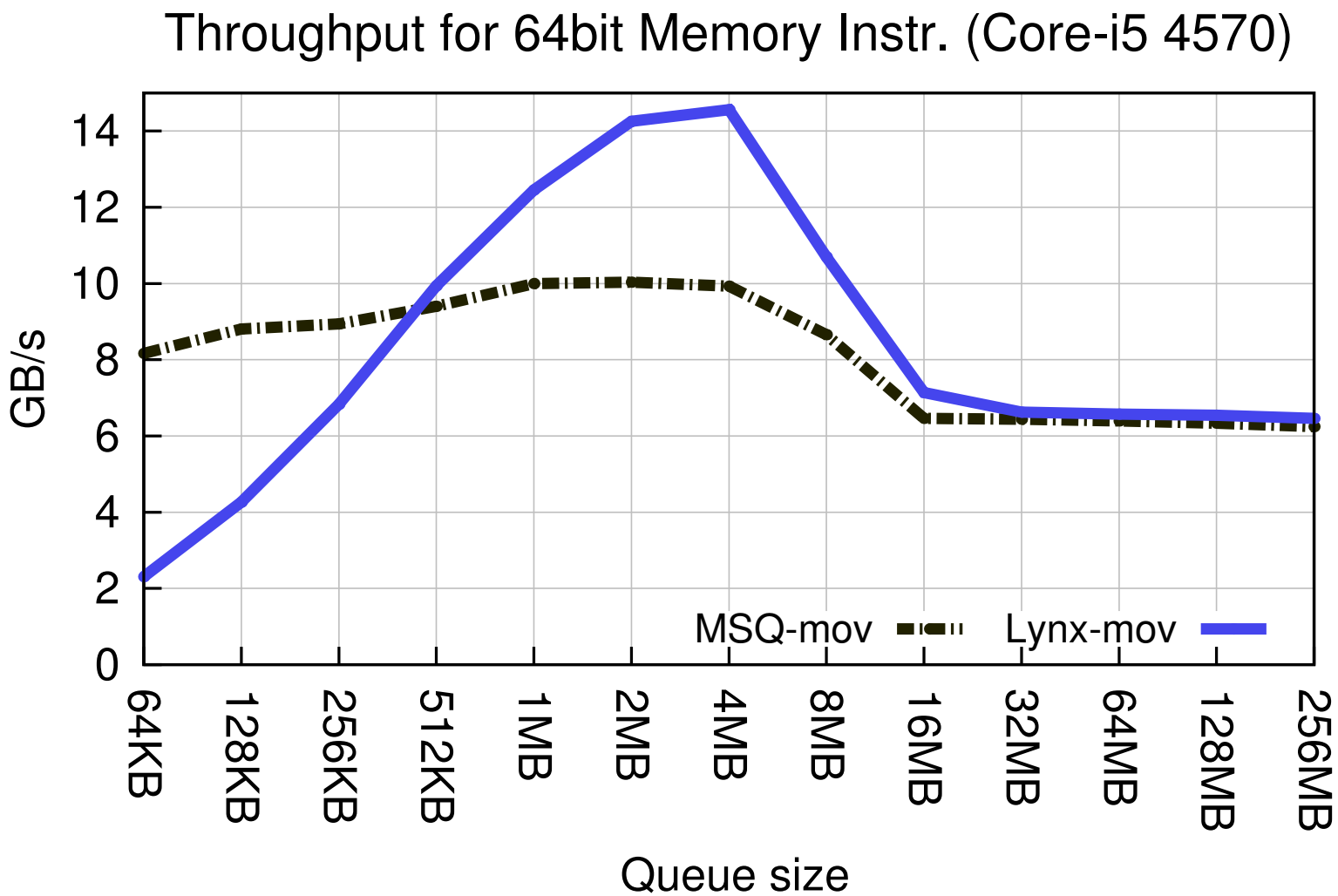
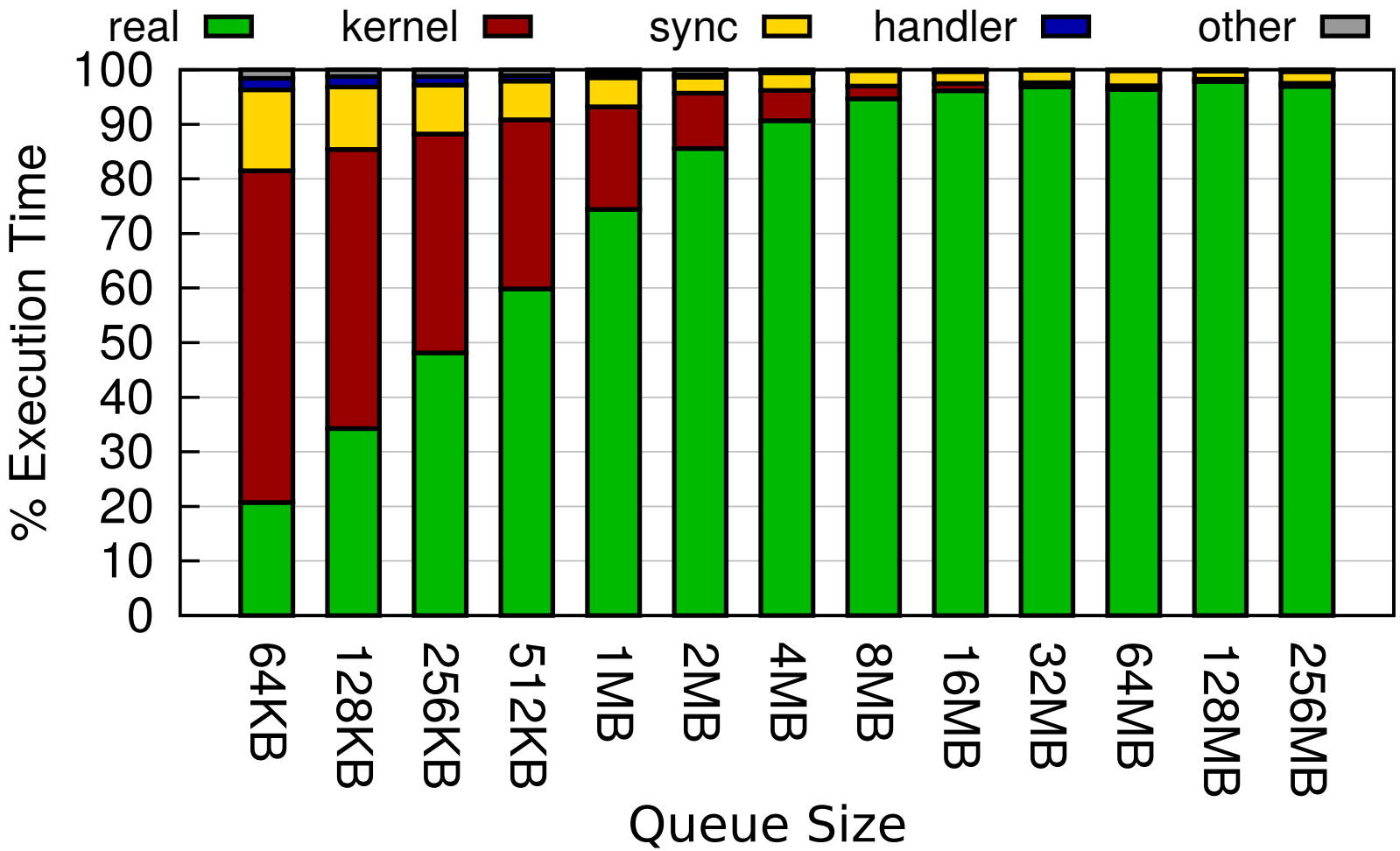
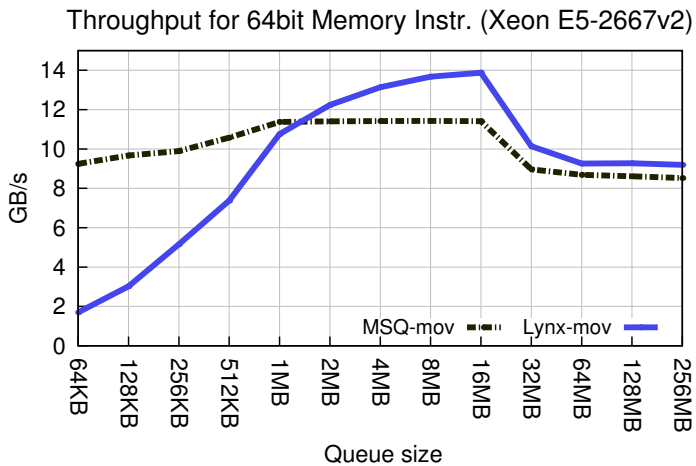
Throughput (GB/s) on Intel core-i5

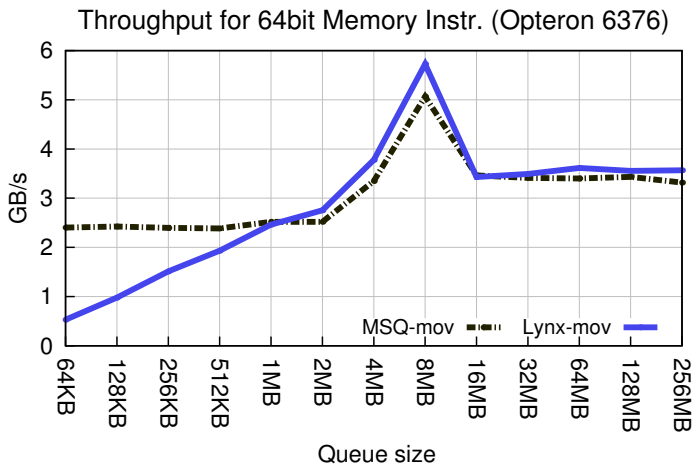


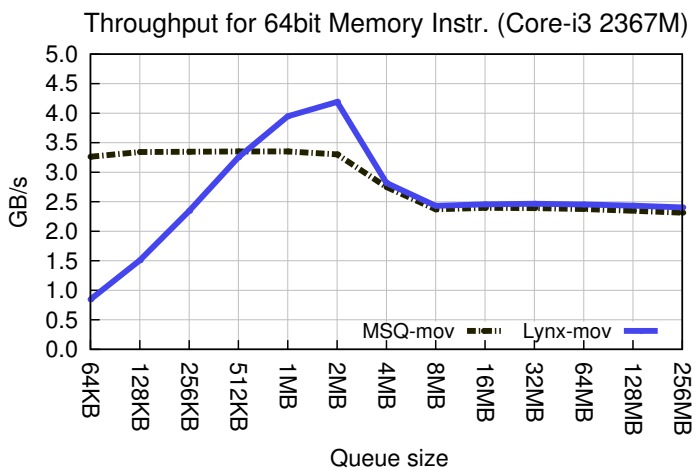
Breakdown of Lynx Overheads

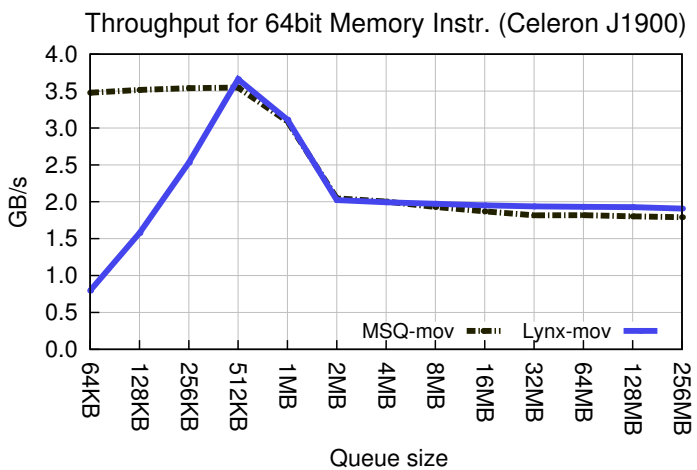


Throughput (GB/s) on Various Machines

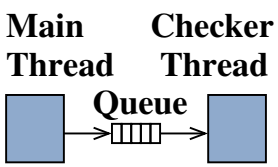


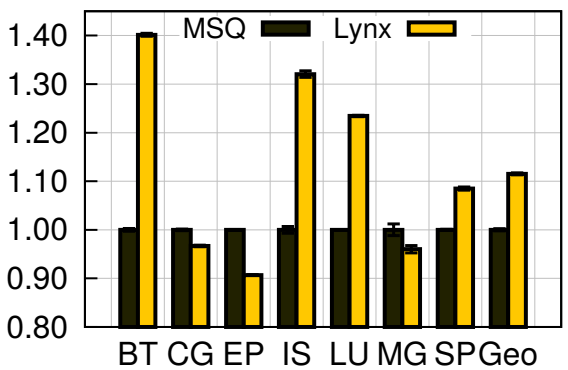




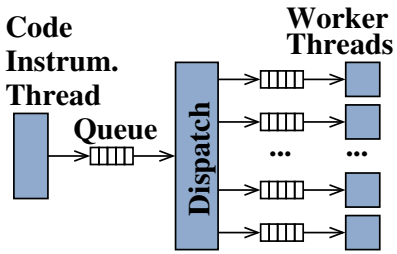


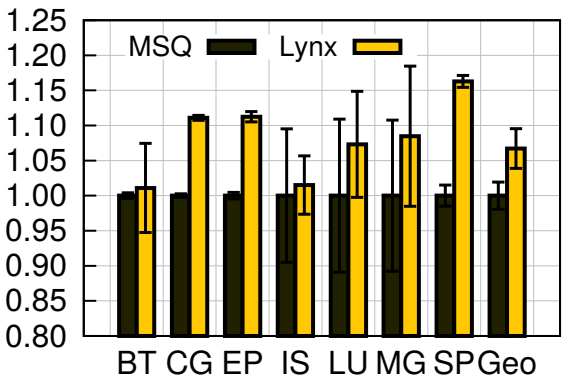
Real World Applications on Intel Xeon



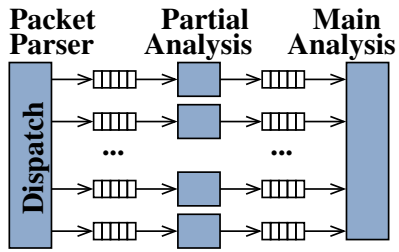


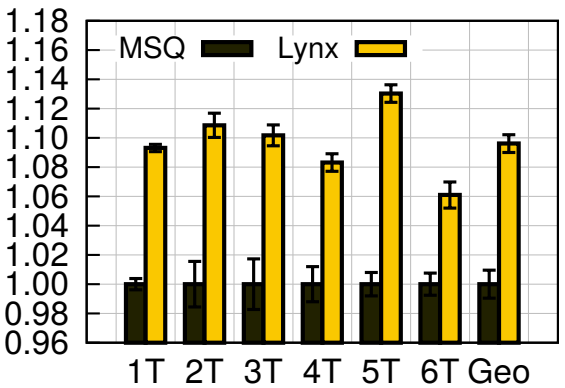
SRMT





SD3





NetworkAnalyser

- The best queue configuration with Lynx is better than the best with MSQ

Conclusion

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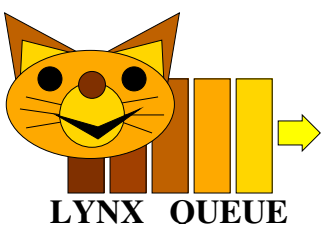
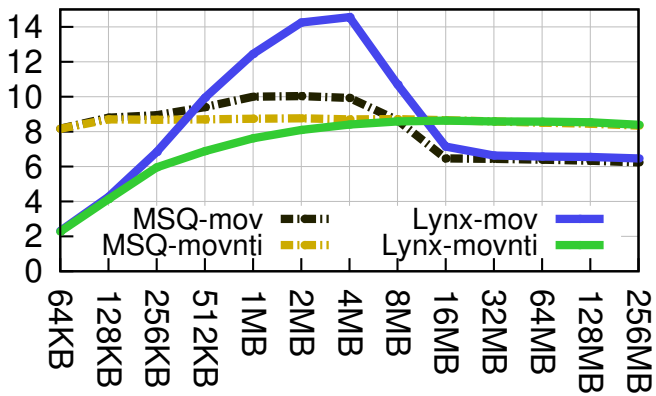
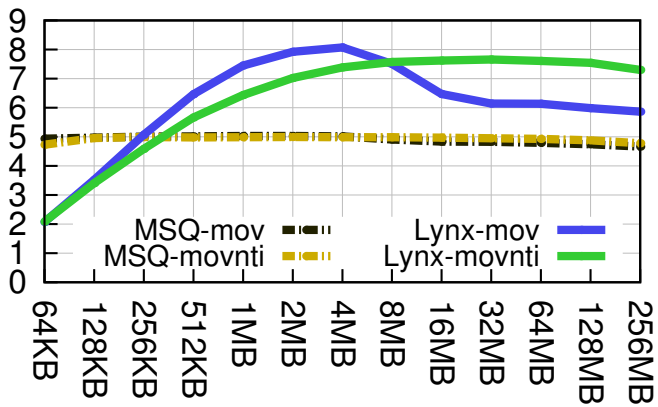
`https://www.cl.cam.ac.uk/~km647/papers/lynx/lynxQ.tar.bz2`

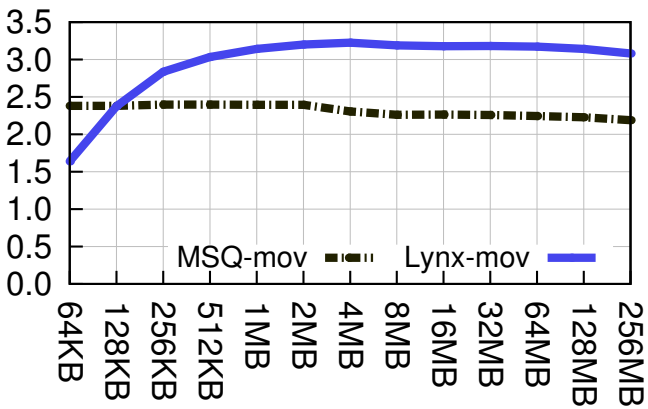


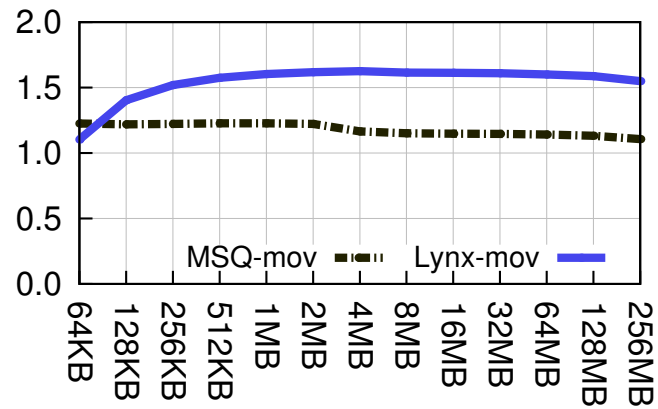
Back-up slides

Throughput (GB/s) on Intel core-i5









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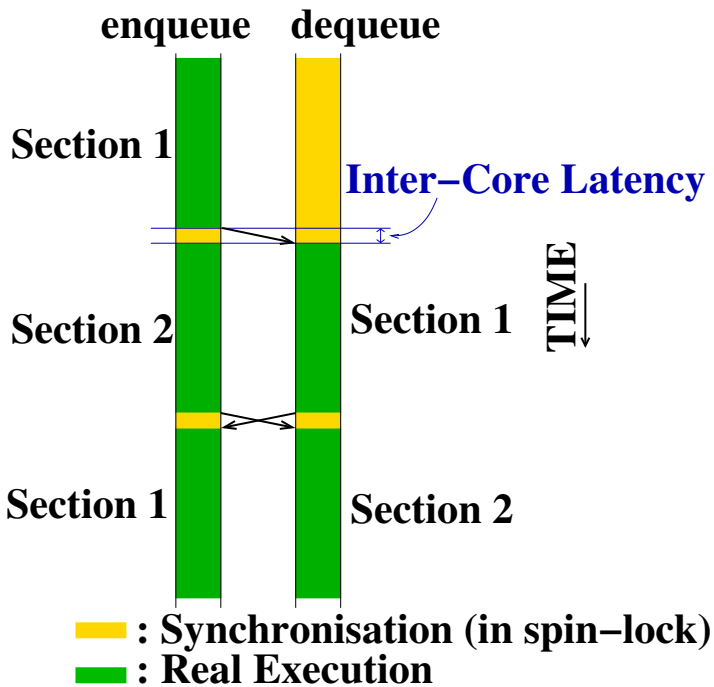
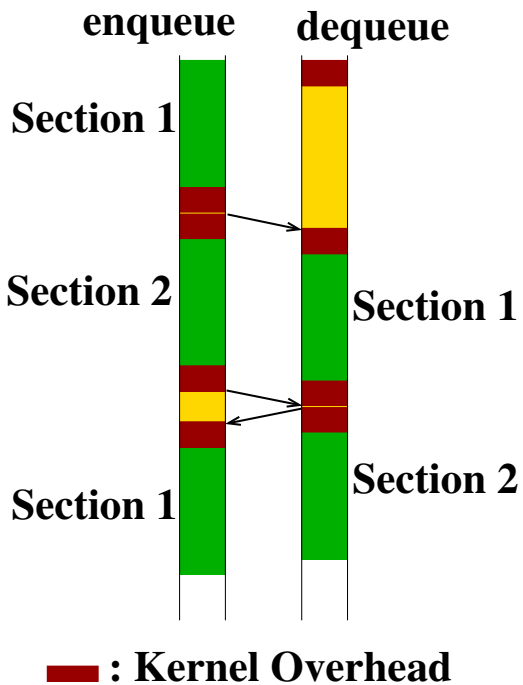
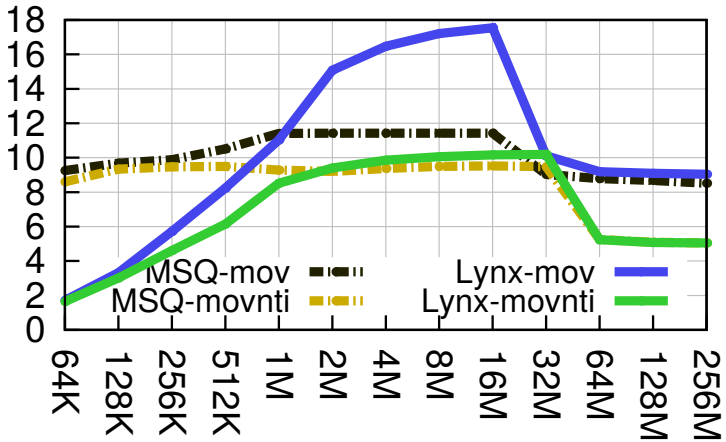
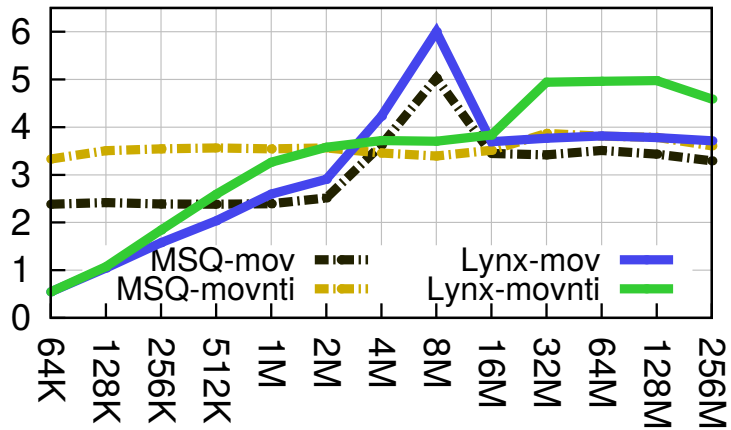




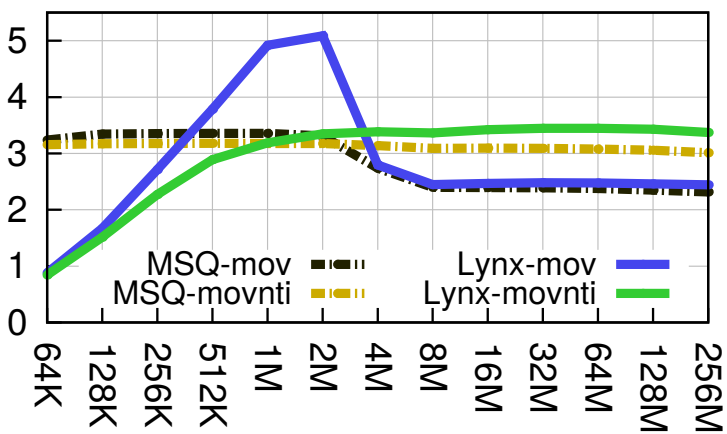
Throughput (GB/s) on Different Machines



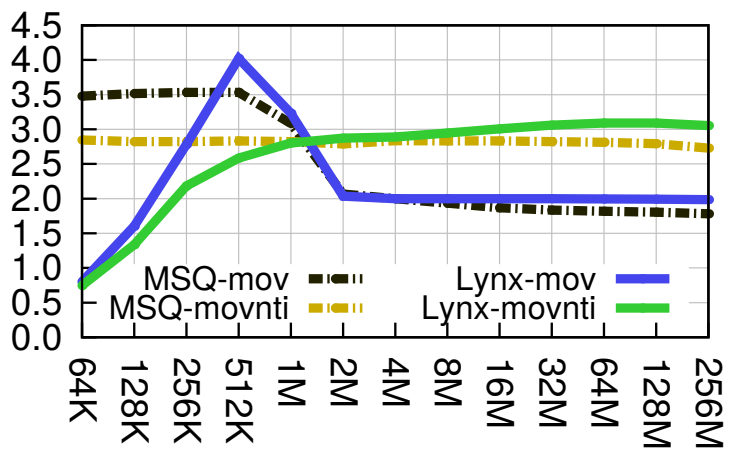
Intel Xeon E5-2667 v2



AMD Opteron 6376



Intel Core-i3 2367M



Intel Celeron J1900